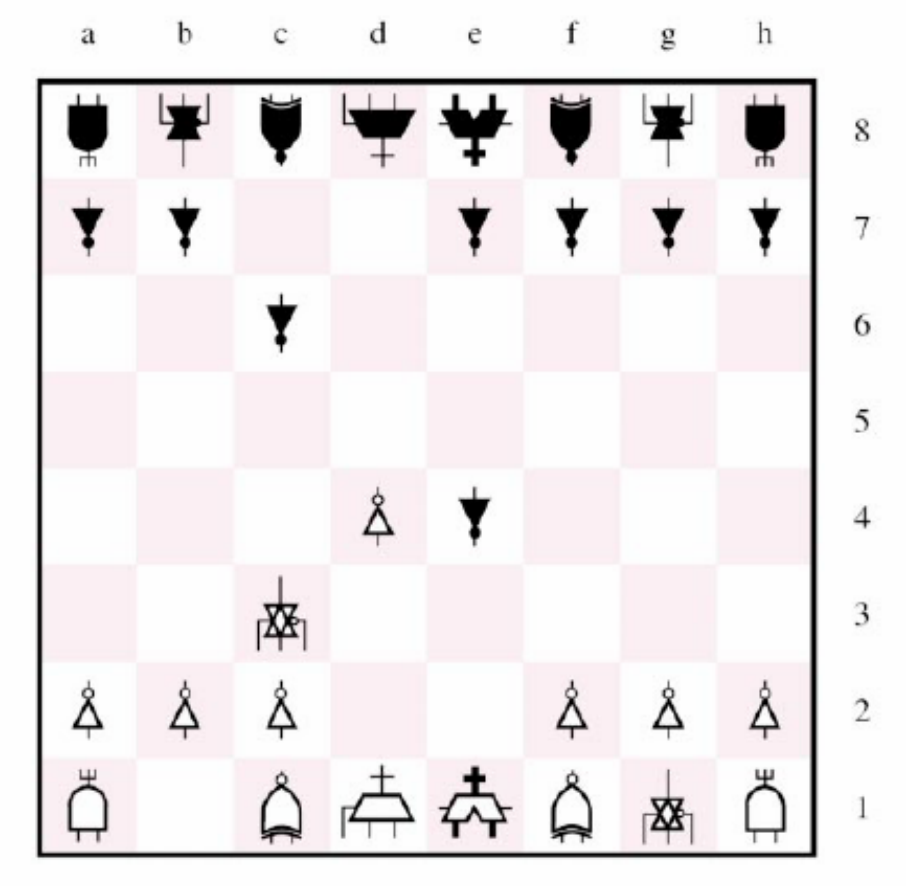
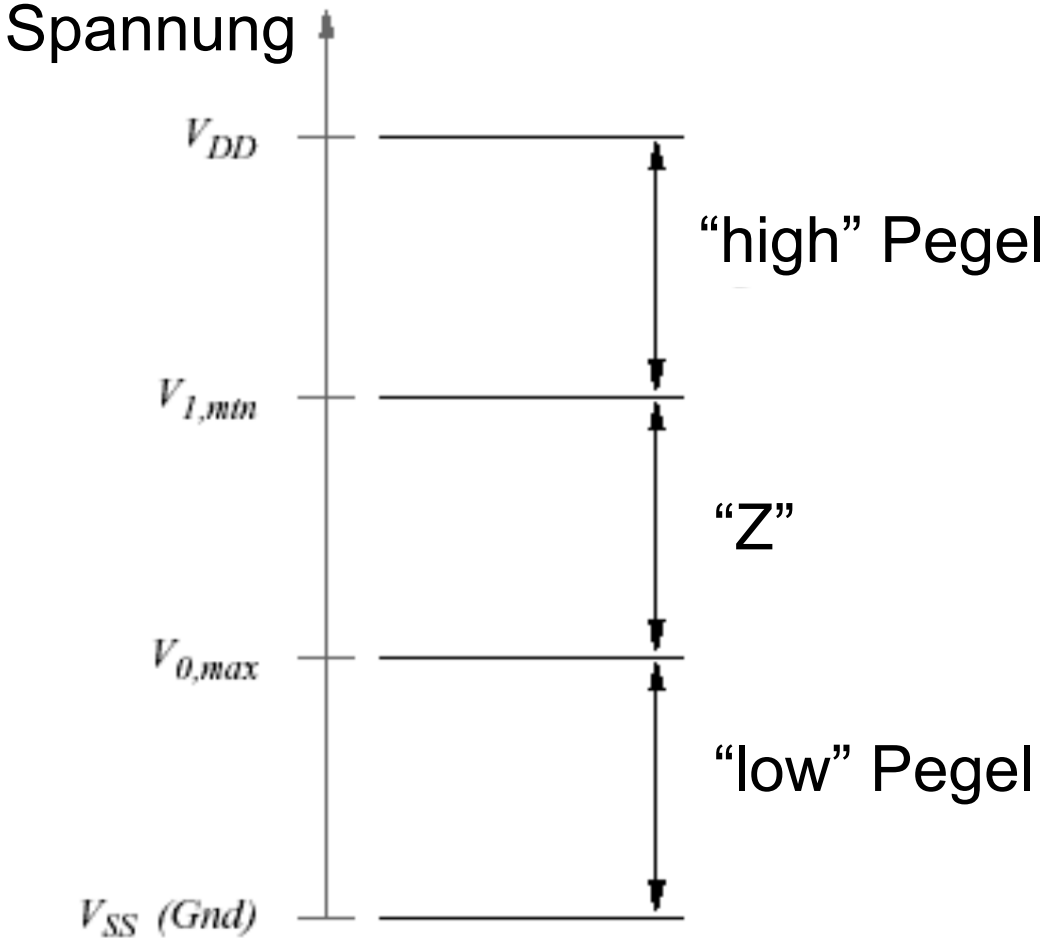
Programmierbare Logikbausteine



Übersicht über verschiedene PLD - Architekturen, Systematisierung

Einführung

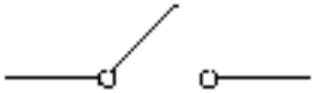


$V_{0,max} = 40\%V_{DD}$ und $V_{1,max} = 60\%V_{DD}$

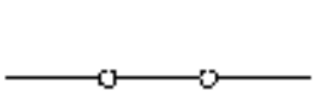
NMOS

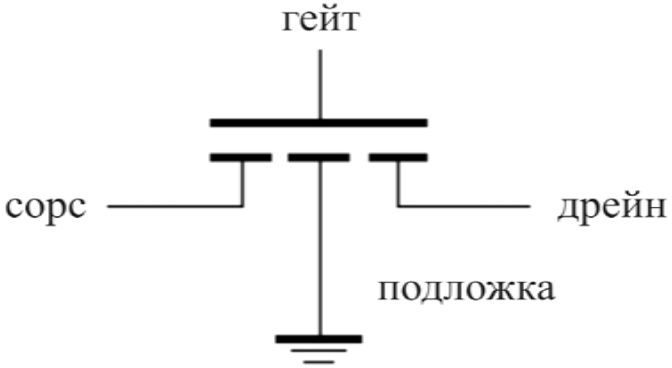
MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor)

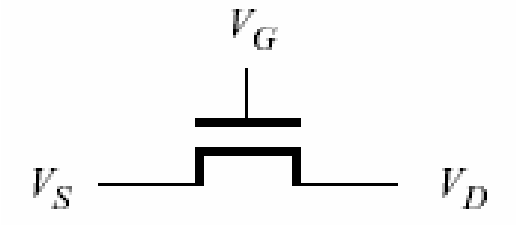
x = “low” Pegel



x = “high” Pegel



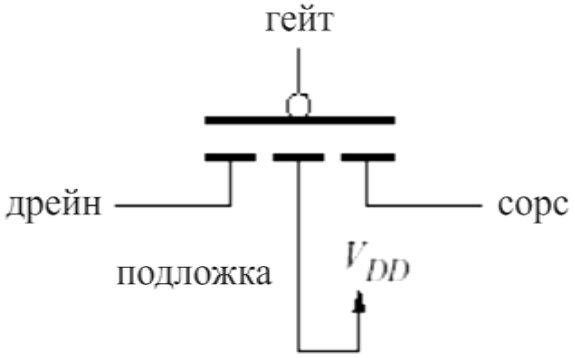


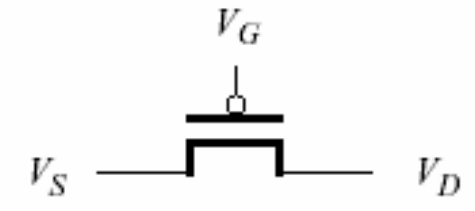


PMOS

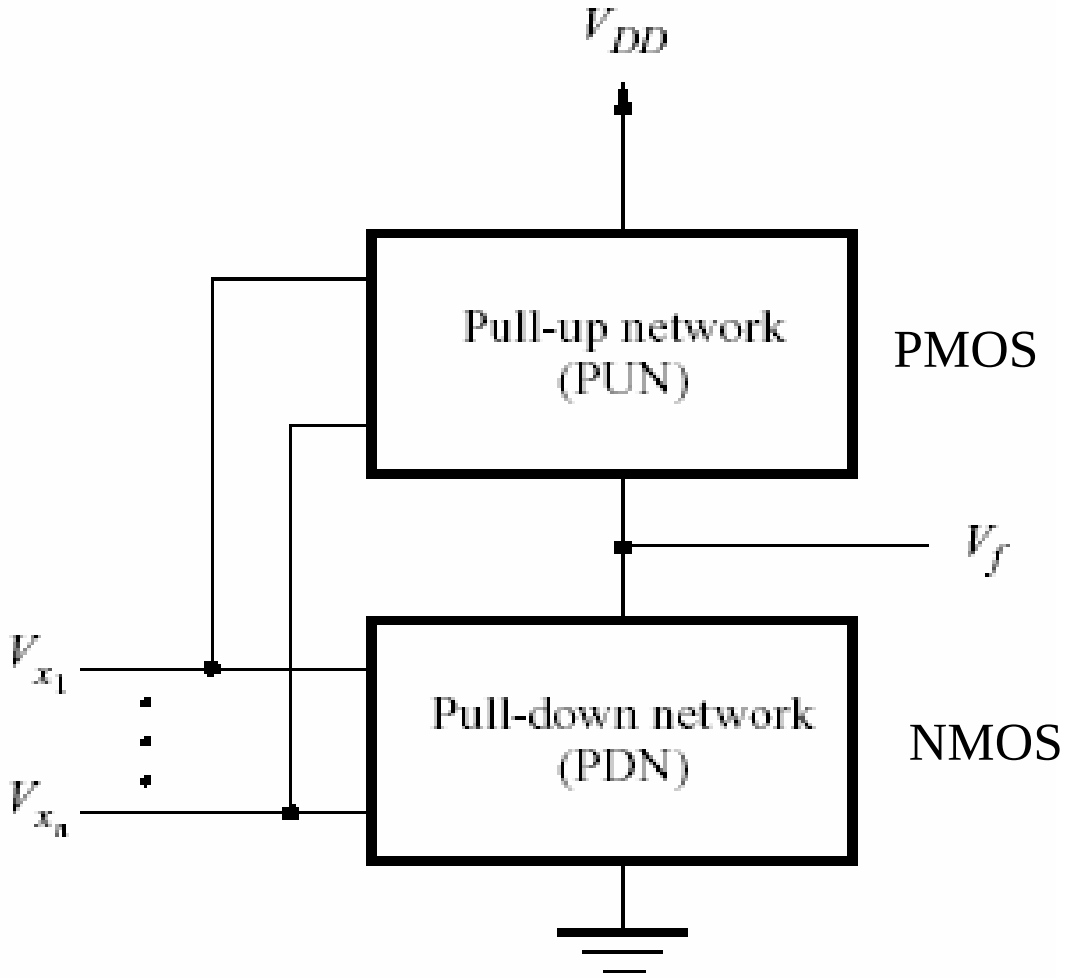
x = “high” Pegel

x = “low” Pegel



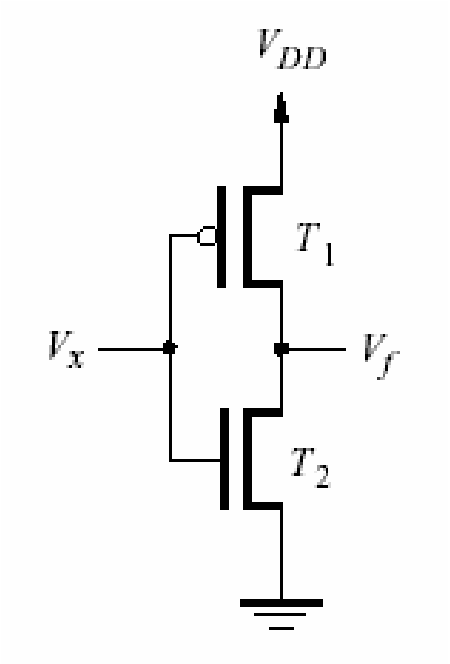


CMOS Technologie (Complementary-Metal-Oxide-Semiconductor)



NOT Schaltung

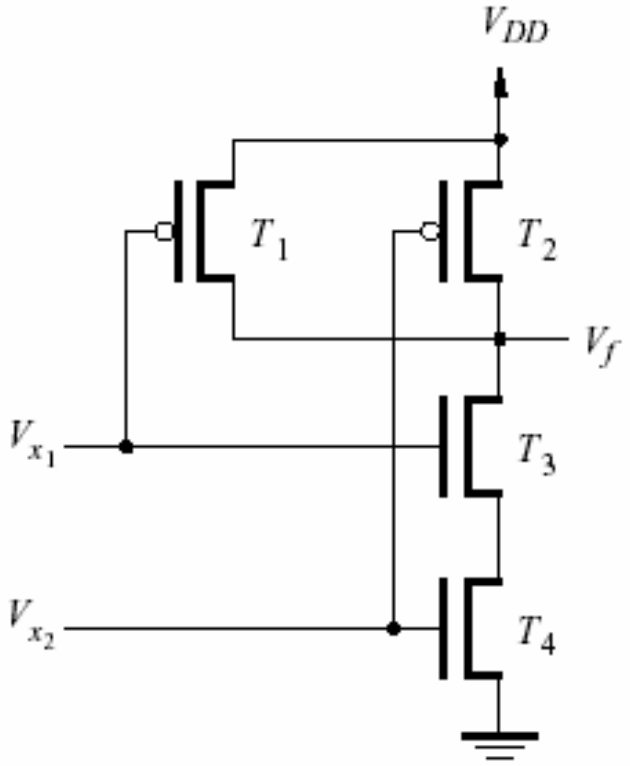
Schaltbild



Wahrheitstabelle

x	T_1 T_2	f
0	on off	1
1	off on	0

NAND Schaltung



$$f = (x_1.x_2)' = \overline{x_1.x_2}$$

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	**on**	**on**	**off**	**off**	1
0	1	**on**	**off**	**off**	**on**	1
1	0	**off**	**on**	**on**	**off**	1
1	1	**off**	**off**	**on**	**on**	0

De Morgan's Law

$$\left[f\left(x_1, x_{2,}, \ldots, x_n, 0, 1, +, *\right)\right]' = f\left(x_1', x_2', \ldots, x_n', 1, 0, *, +\right)$$

PUN $\quad f = \overline{x_1 . x_2} = \left(x_1 . x_2\right)' = x_1' + x_2' = \overline{x_1} + \overline{x_2}$

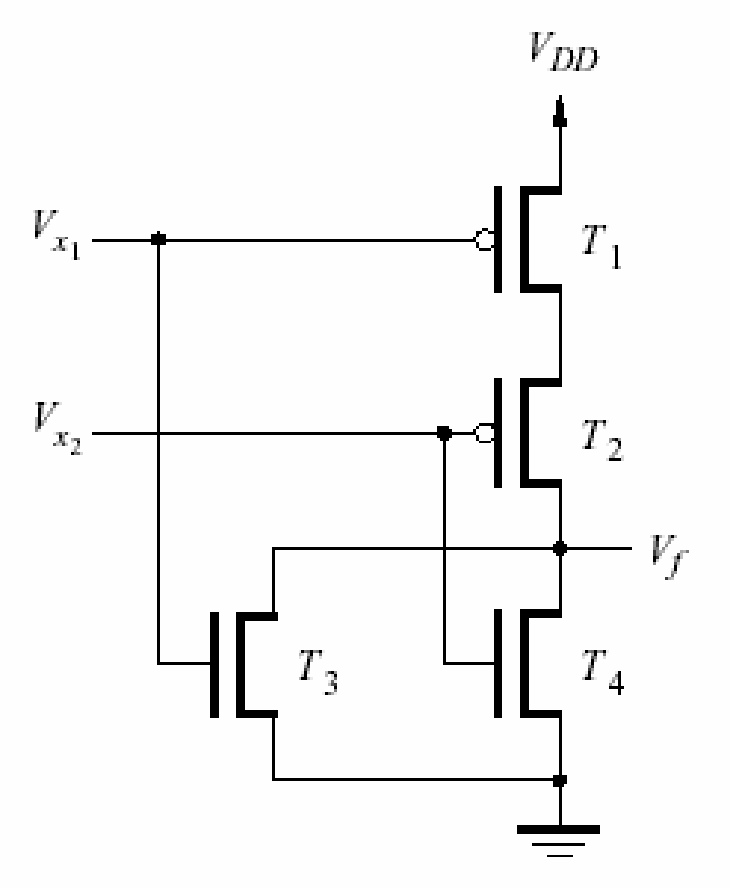
PDN $\quad \overline{f} = \overline{\overline{x_1 . x_2}} = x_1 . x_2$

NOR (NOT OR) Schaltung ???

PUN $f = \overline{x_1 . x_2} = (x_1 + x_2)' =$

PDN $\overline{f} = \left(\overline{x_1 + x_2}\right)' =$

NOR (NOT OR) Schaltung



Minterms and sum of products

m	A	B	C	F_0	F_1	F_2	F_3
0	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
2	0	1	0	0	1	1	1
3	0	1	1	0	1	0	1
4	1	0	0	1	1	0	0
5	1	0	1	0	0	0	1
6	1	1	0	1	1	1	1
7	1	1	1	0	1	0	1

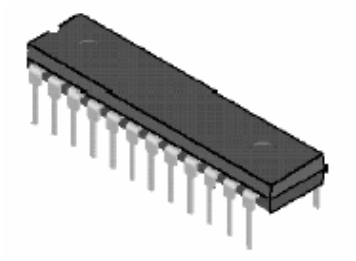
$$F_0 = \sum m(0,1,4,6) =$$
$$= A'B'C' + A'B'C + AB'C' + ABC' =$$
$$= A'B'(C' + C) + AC'(B' + B) =$$
$$= A'B' + AC'$$

$$F_1 = \sum m(2,3,4,6,7) = B + AC'$$

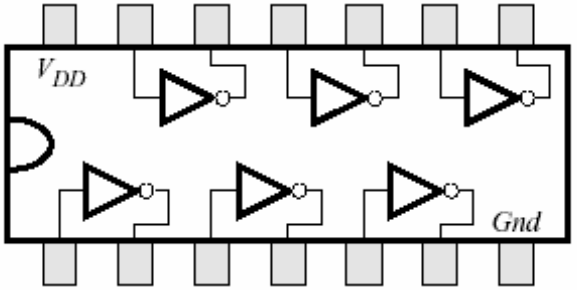
$$F_2 = \sum m(0,1,2,6) = A'B' + BC'$$

$$F_3 = \sum m(2,3,5,6,7) = AC + B$$

74XX Series



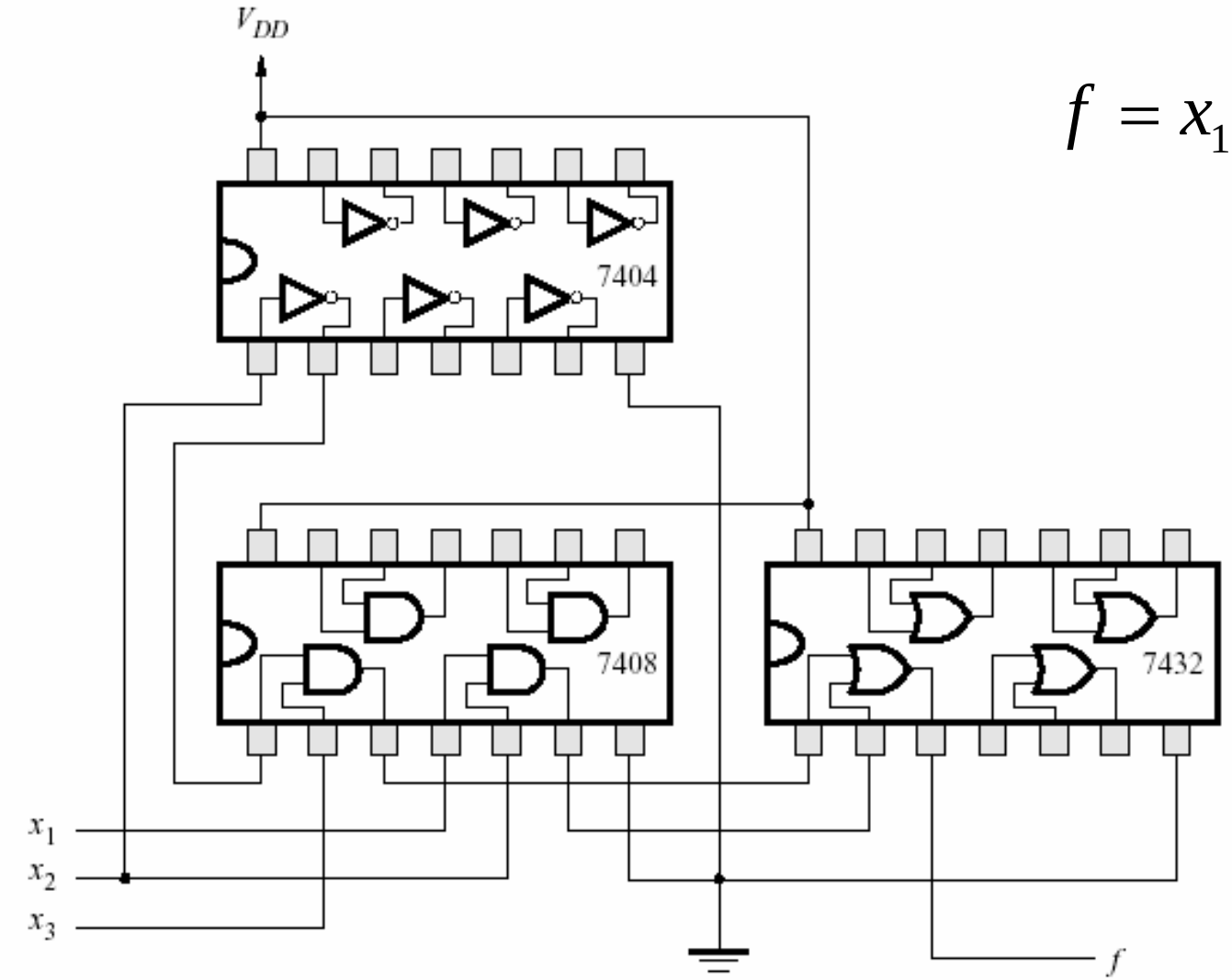
DIP (Dial-In-line-Package)



7404

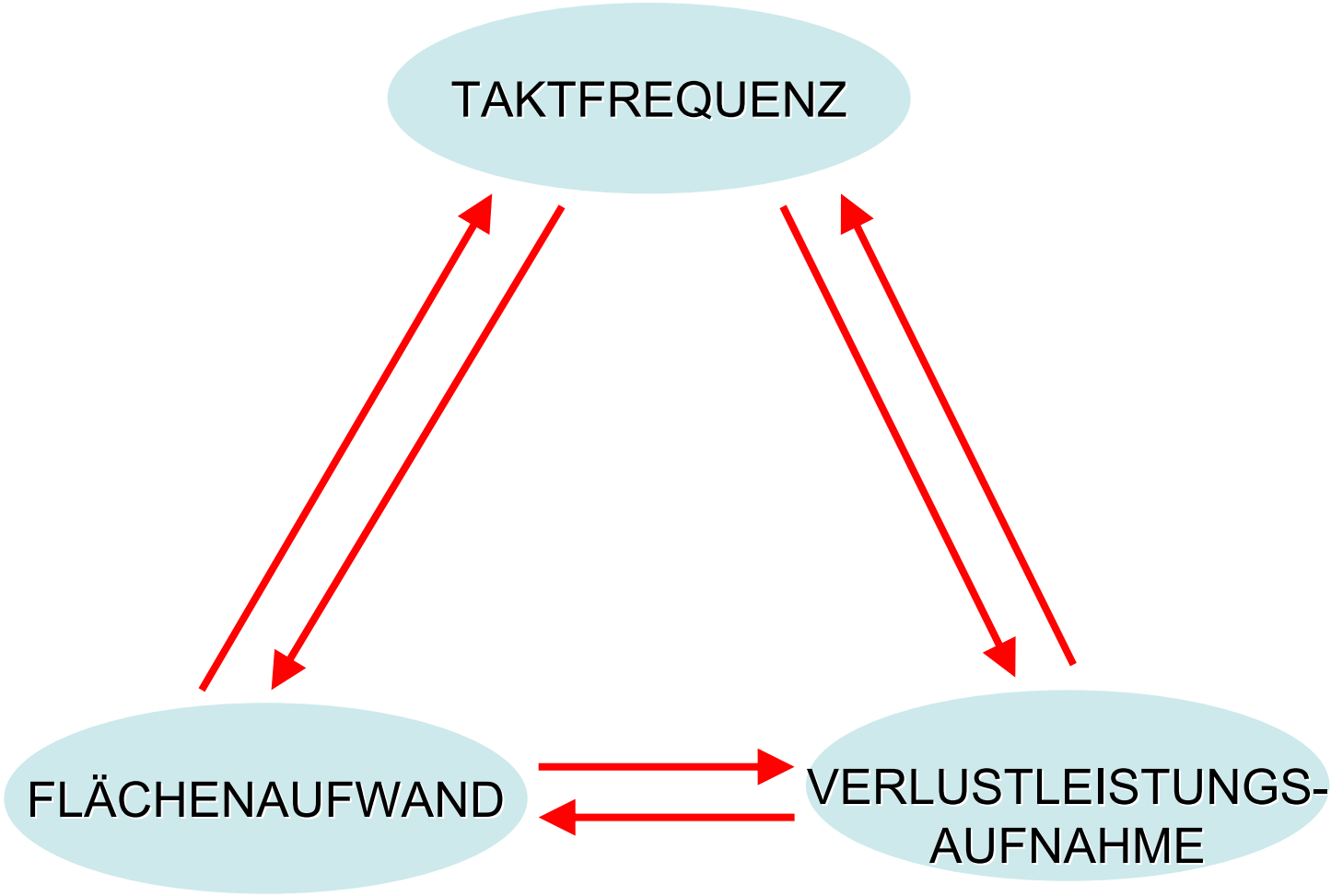
74LS00 - Transistor-Transistor-Logic, TTL;
74HC00 - CMOS

74XX Series



$$f = x_1.x_2 + \overline{x_2}.x_3$$

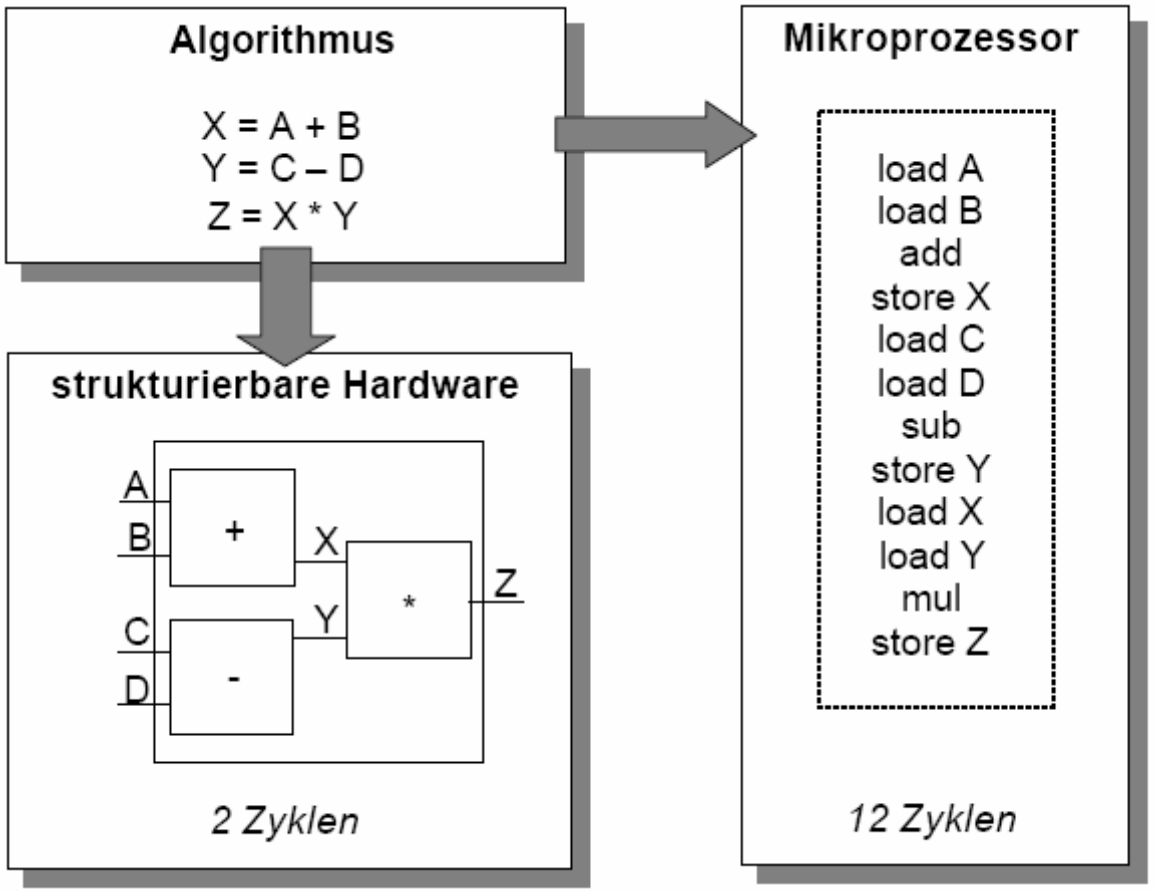
Dreieck beim Entwurf integrierter Digitalschaltungen



Verlustleistung

$$P_{\text{Verlustleistungsaufnahme}} = \sum \left[\begin{array}{c} \text{Anzahl der} \\ \text{Register} \end{array} \right] + \left[\text{Taktfrequenz} \right] + \left[\begin{array}{c} \text{Prozentsatz} \\ \text{an logischen} \\ \text{Gattern} \end{array} \right]$$

Computing in Space vs. Computing in Time



Computing in Space vs. Computing in Time

Räumliche Sequentialisierung

- Datenflussorientierung

- Parallelisierung (Addition und Subtraktion)

- Pipelining (Add/Sub und Mul)

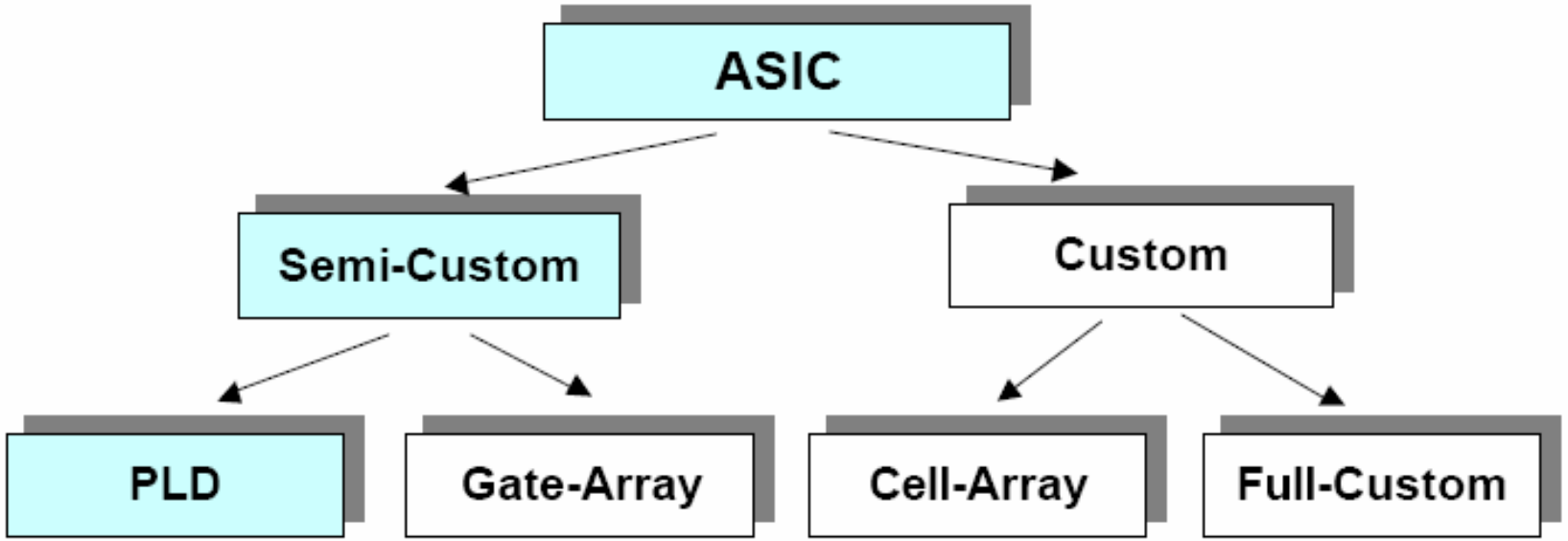
Zeitliche Sequentialisierung

- Kontrollflussorientierung

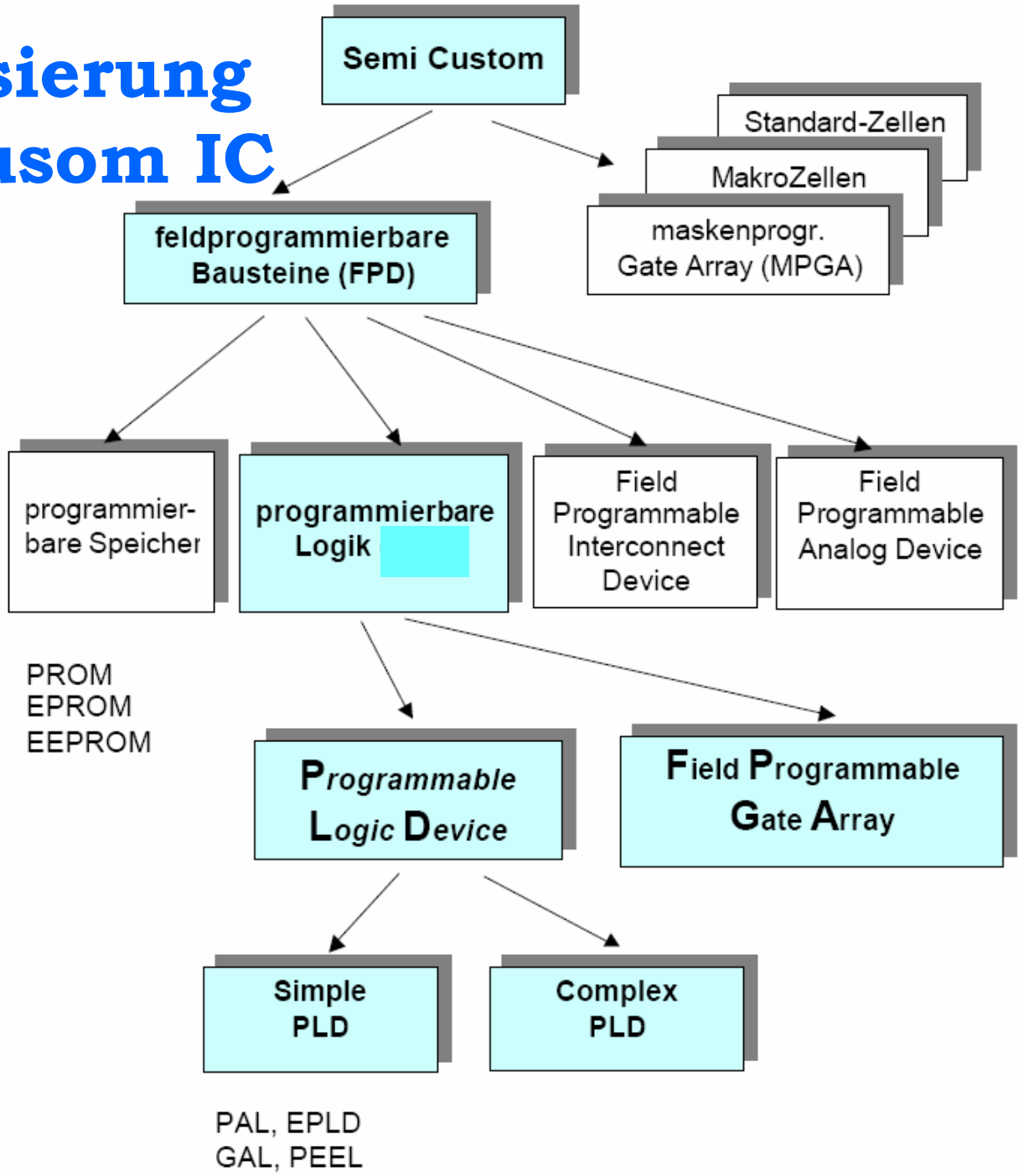
- Pipelining bei modernen Mikroprozessoren (DSP) auch möglich

Vergleich PLD mit anderen Entwurfsmethoden

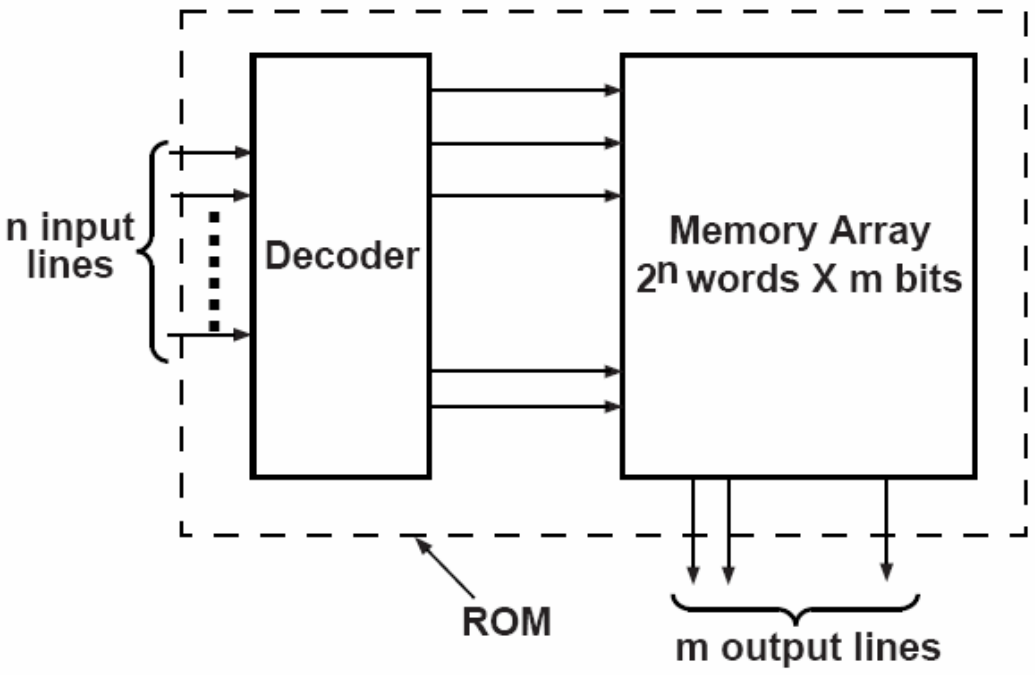
ASIC – Kundenspecifische Schaltkreise



Systematisierung der Semi-Cusom IC



Basic ROM Structure



- Conceptually ROM consists of a decoder and memory array;

- 2^n x m ROM → m functions of n input variables (can store truth table with 2^n rows and m columns) – implementing combinatorial logic

Type of ROMs

There are 4 different ways of programming:

- **Mask programming**: done by the semiconductor company during the last fabrication process. Economical if large quantity is made;

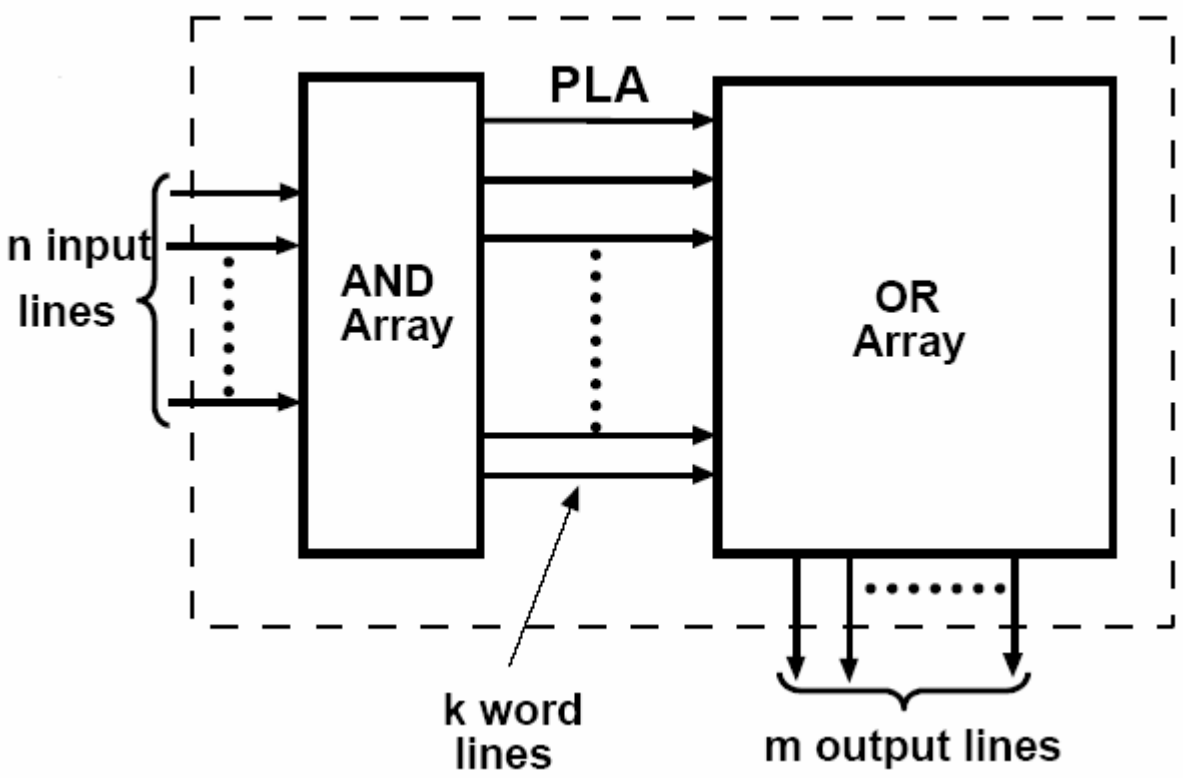
- **PROM (Programmable ROMs):** PROM unit contains all the fuses intact giving all 1's in the bits of stored words. The fuses are blown by application of high-voltage pulse to the device through a special pin. A blown fuse defines a binary 0 state. This is an irreversible process. PROM programmers are available for this purpose.

Type of ROMs

- **Erasable PROM** – same as PROM but can be restructured to the initial state even though it has been programmed previously. When EPROM is placed under special ultra-violet light for a given period of time, the short wave radiation discharges internal floating gates that serve as the programmed connections (initialization);

- **Electrically-erasable PROM (E^2PROM):** same as EPROM except that erasing can be done with an electrical signal instead of ultra-violet light. The advantage is that the device can be erased without removing it from its socket.

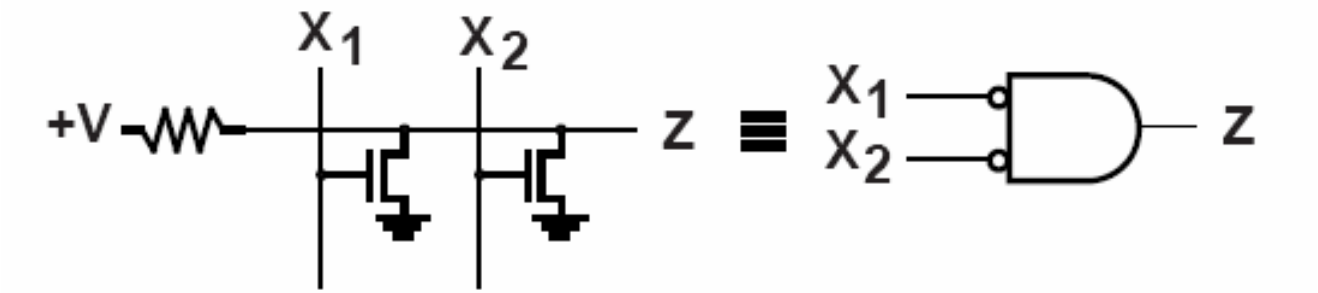
Programmable Logic Array Structure



- *m* functions of *n* input variables;
- decoder → AND array;
- OR array → OR together product term needed to form output function

nMOS NOR Gate

Logical gates are formed in array by connecting nMOS switching transistors between the column lines and the row lines.

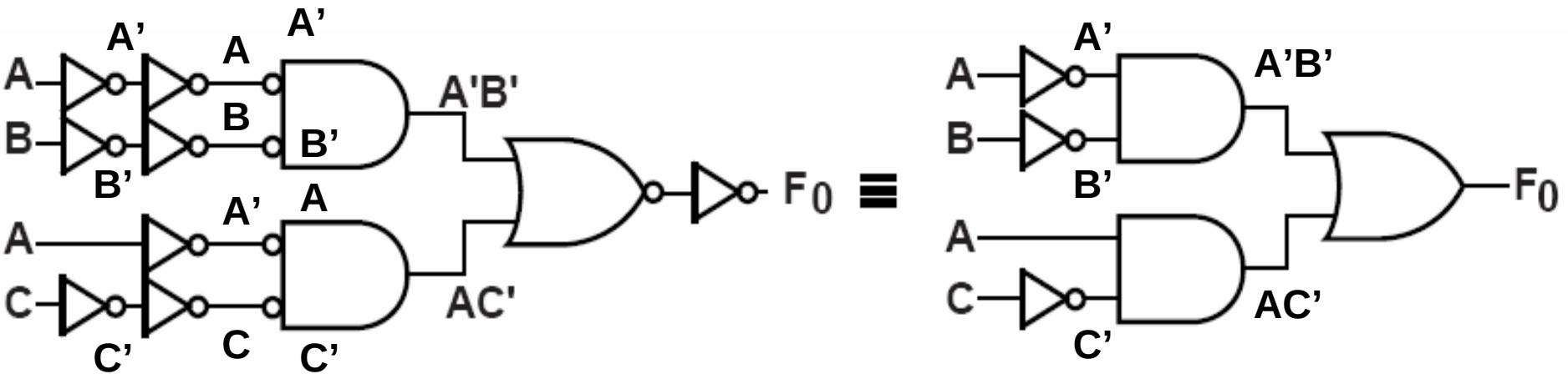


X_1	X_2	nMOS	Z
0	0	off, off	1
0	1	off, on	0
1	0	on, off	0
1	1	on, on	0

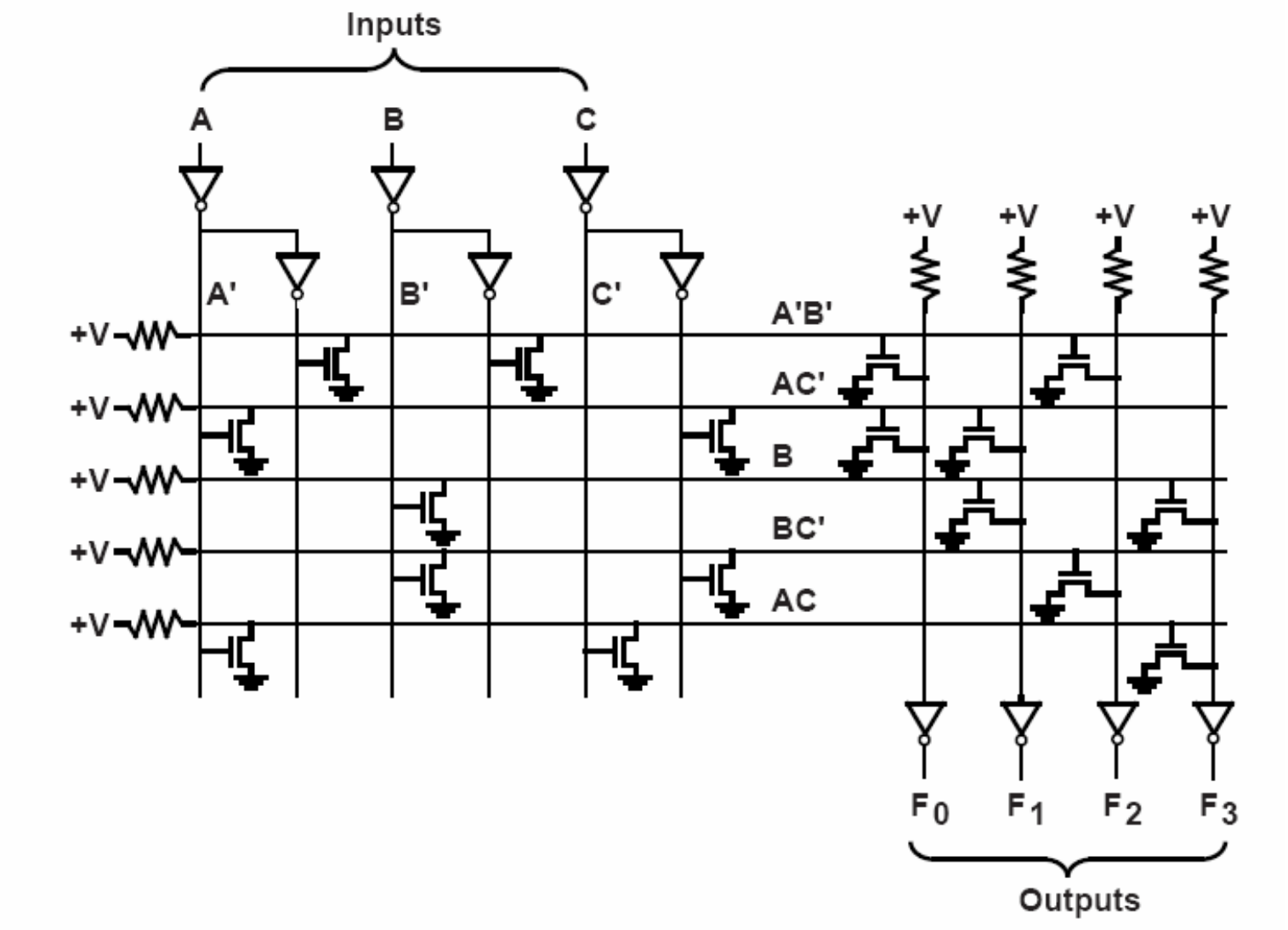
$Z = X_1' X_2' = (X1 + X2)' =$
$=$ *NOT-OR (NOR) Gate*

NOR-NOR Logic

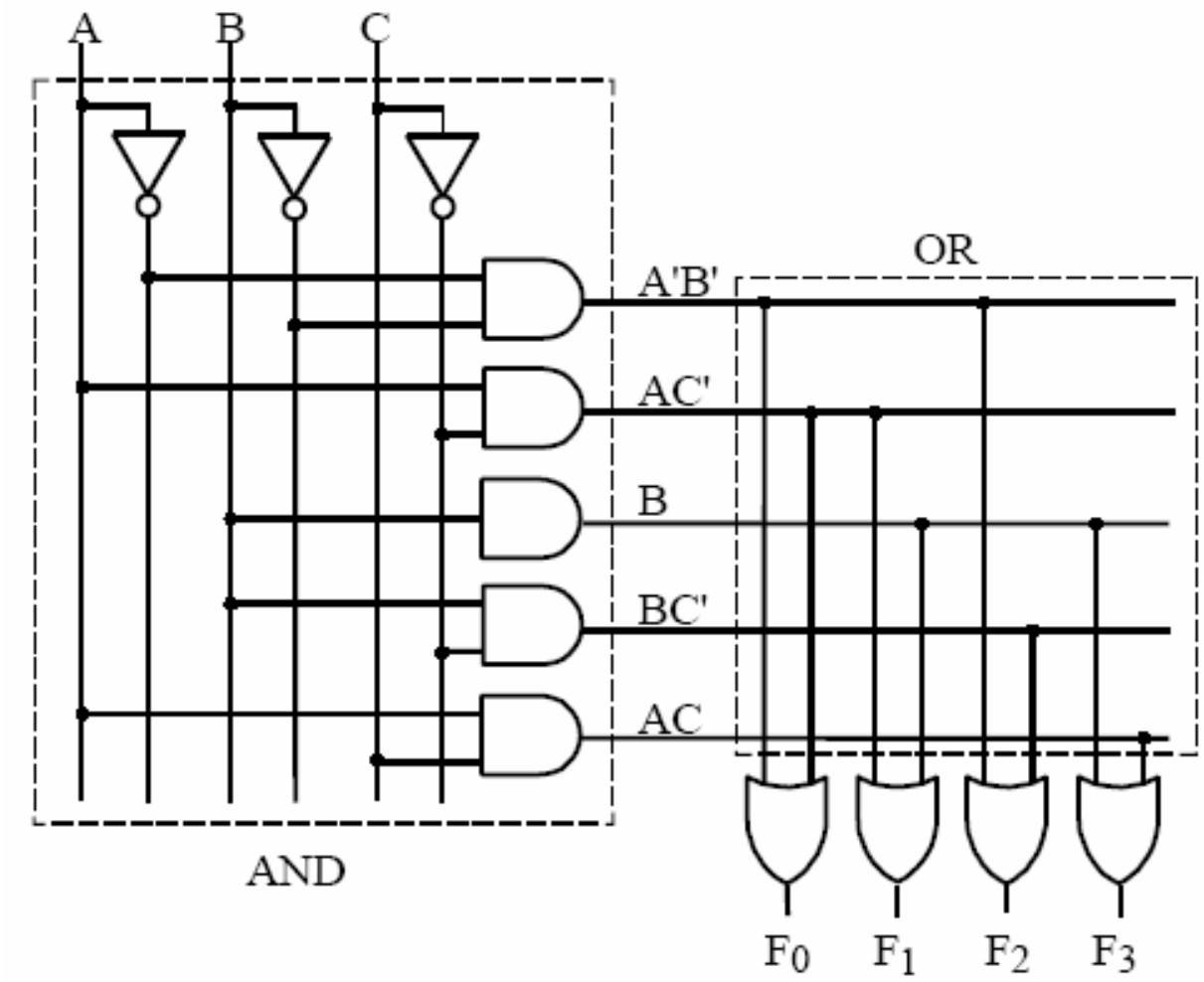
$$F_0 = \sum m(0,1,4,6) = A'B' + AC'$$



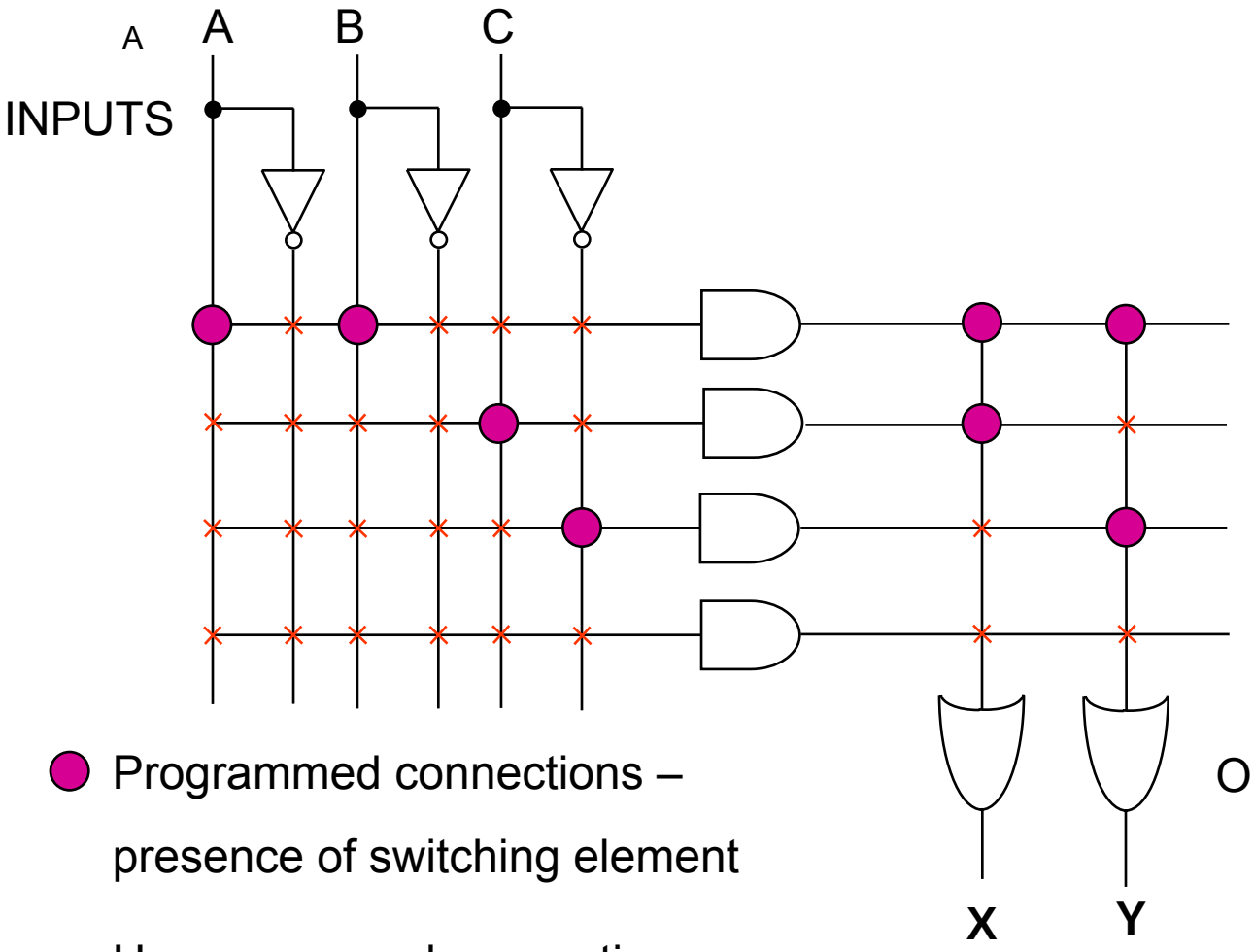
nMOS PLA



AND-OR PLA



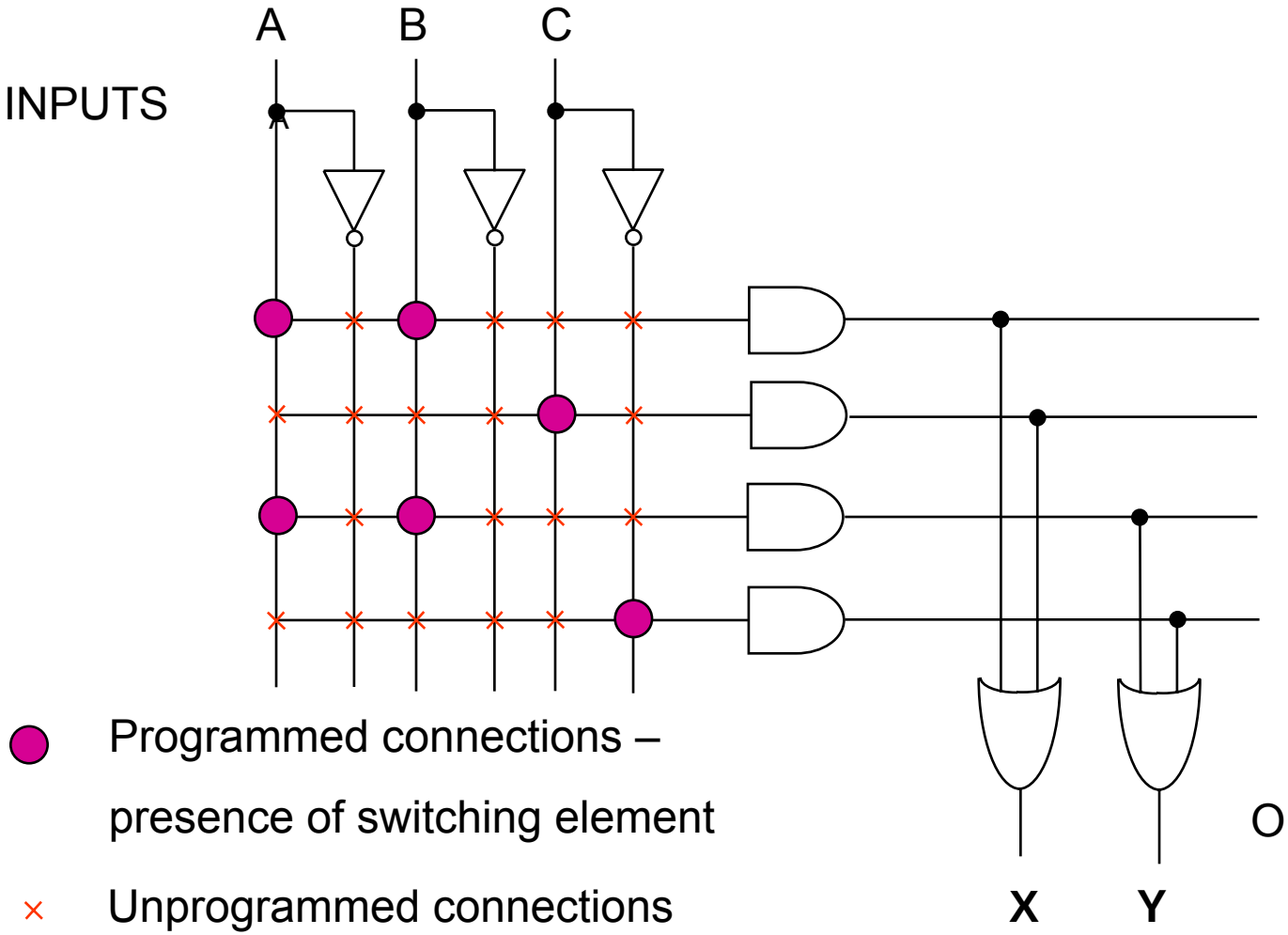
Programmable Logic Array - PLA



X = A & B # C
Y = A & B # !C

- ● Programmed connections – presence of switching element
- × Unprogrammed connections

Programmable Array Logic - PAL

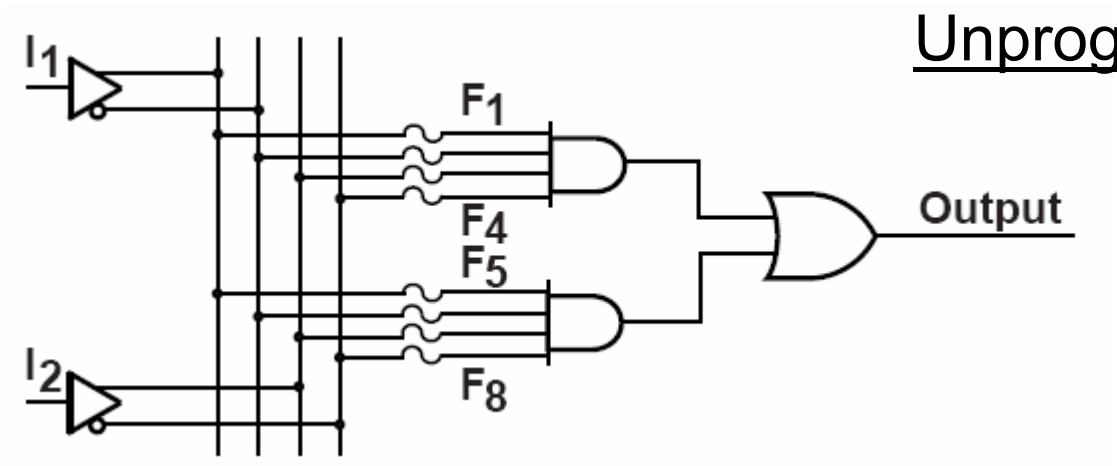


● Programmed connections – presence of switching element

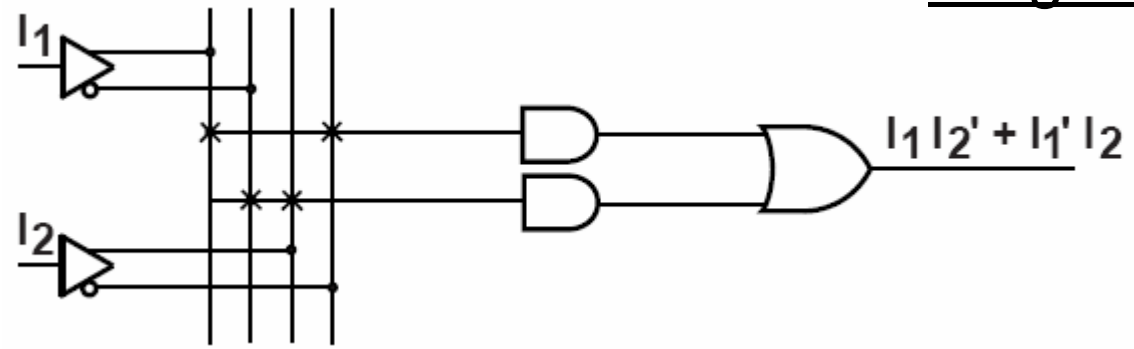
× Unprogrammed connections

Programmable Array Logic - PAL

Unprogrammed PAL segment



Programmed PAL segment



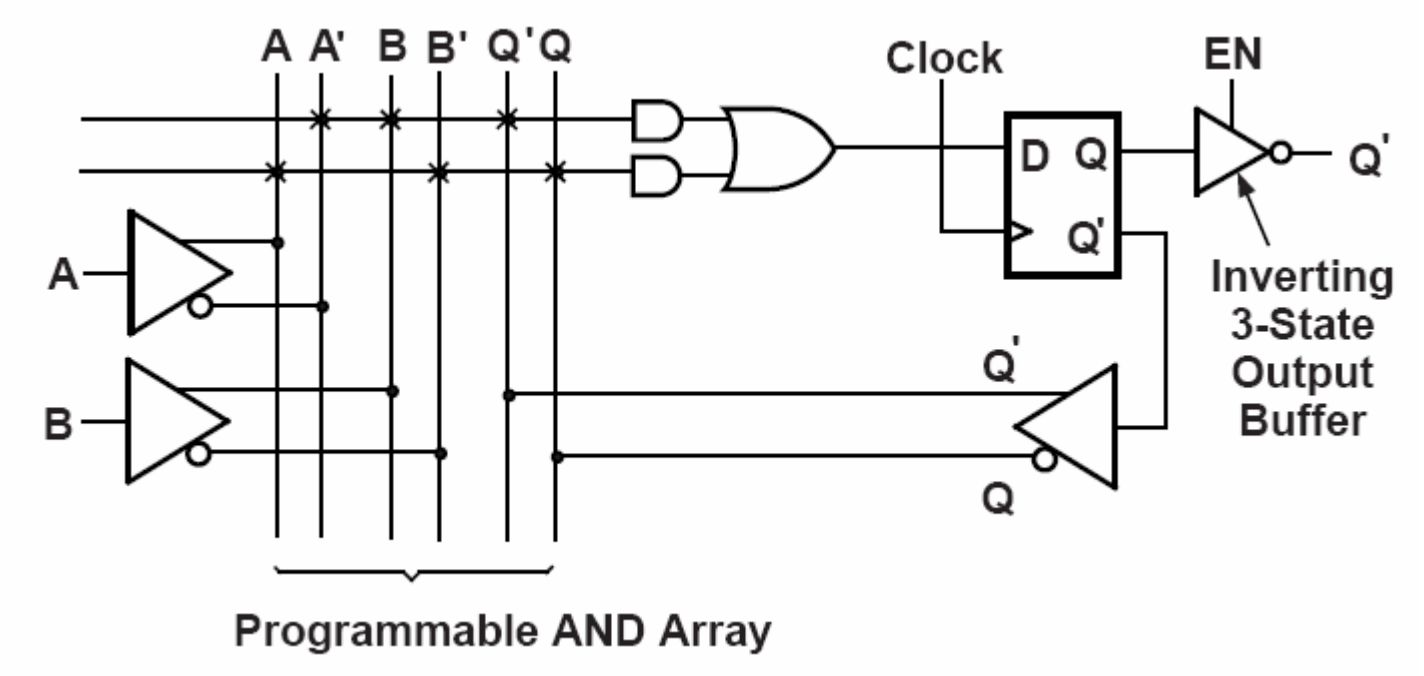
Sequential Programmable Devices

- Digital systems are designed using flip-flops and gates. Since the combinatorial PLD consists of only gates, it is necessary to include external flip-flops when they are used in design;
- Sequential programmable devices include both gates and flip flops;
- In this way, the device can be programmed to perform a variety of sequential circuit functions;
- The major types are:
  - Sequential programmable logic devices (***SPLD***)
  - Complex Programmable Logic Device (***CPLD***)
  - Field Programmable Gate Array (***FPGA***)

Sequential Programmable Devices

- Sequential PLD is sometimes referred to as a simple PLD to differentiate it from the complex PLD.
- SPLD includes flip-flops within the integrated circuit chip in addition to the AND-OR array.
- A PAL or PLA is modified by including a number of flip-flops connected to form a register.
- The circuit output can be taken from the OR (combinational output) gates or from the outputs of flip-flops (registered output).
- Additional programmable connections are available to include the flip-flops (D or JK type) outputs in the product terms formed with the AND array.

Sequential Programmable Devices



Realization of the next-state equation:

$$Q^{+} = D = A'BQ' + AB'Q$$

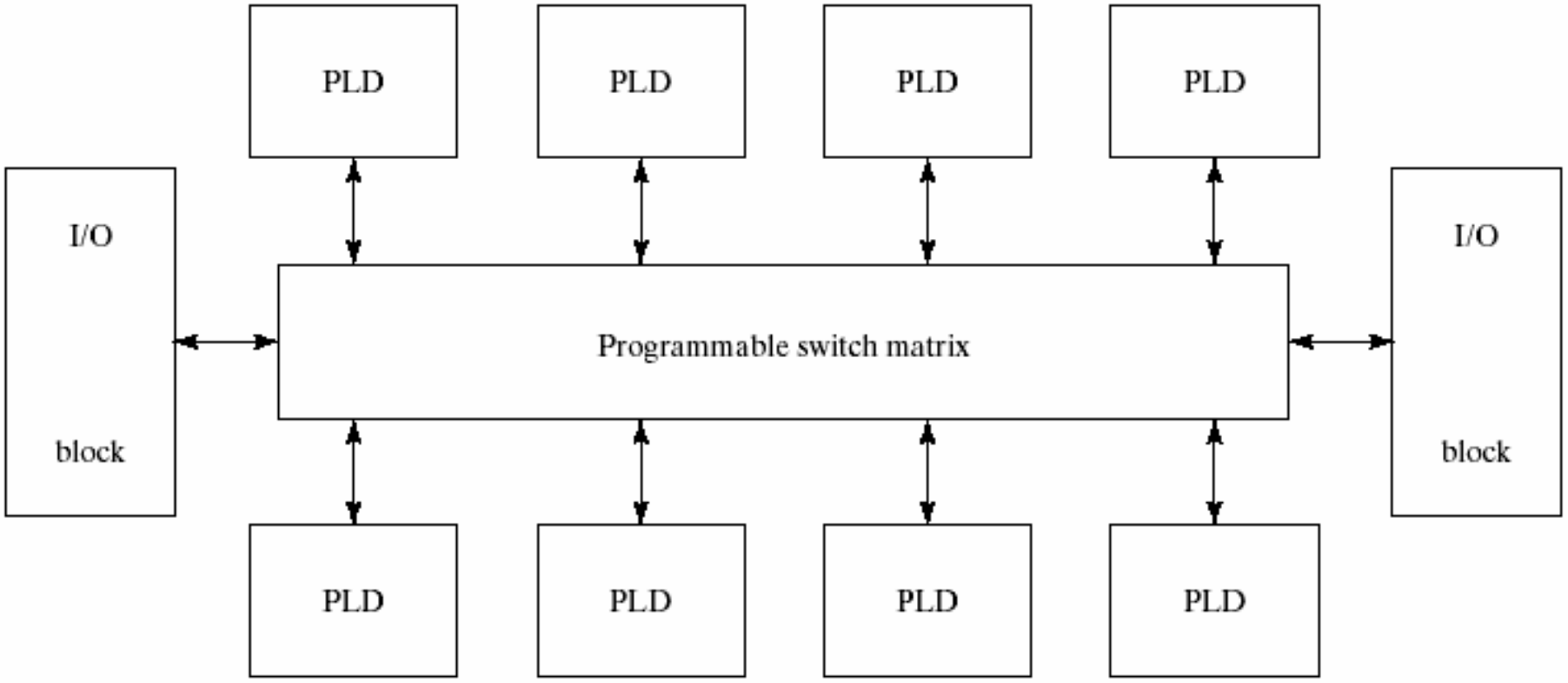
SPLD

- The configuration mostly used for SPLD is the combinatorial PAL together with D flip-flops;
- A PAL that includes flip-flops is referred to as a registered PAL;
- ***Macrocell*** - circuit that contains a sum-of-products combinational logic function and an optional flip-flop;
- A typical SPLD has from 8 to 10 macrocells within one ICE package.

Complex Programmable Logic Devices - CPLD

- The design of a digital system using PLD often requires the connection of several devices to produce the complete specification;
- For these type of applications, Complex Programmable Logic Devices (CPLD) are more suitable;
- A CPLD is a collection of individual PLDs on a single integrated circuit;
- A programmable interconnection structure allows the PLDs to be connected to each other in the same way that can be done with the individual PLD's.

Complex Programmable Logic Devices - CPLD



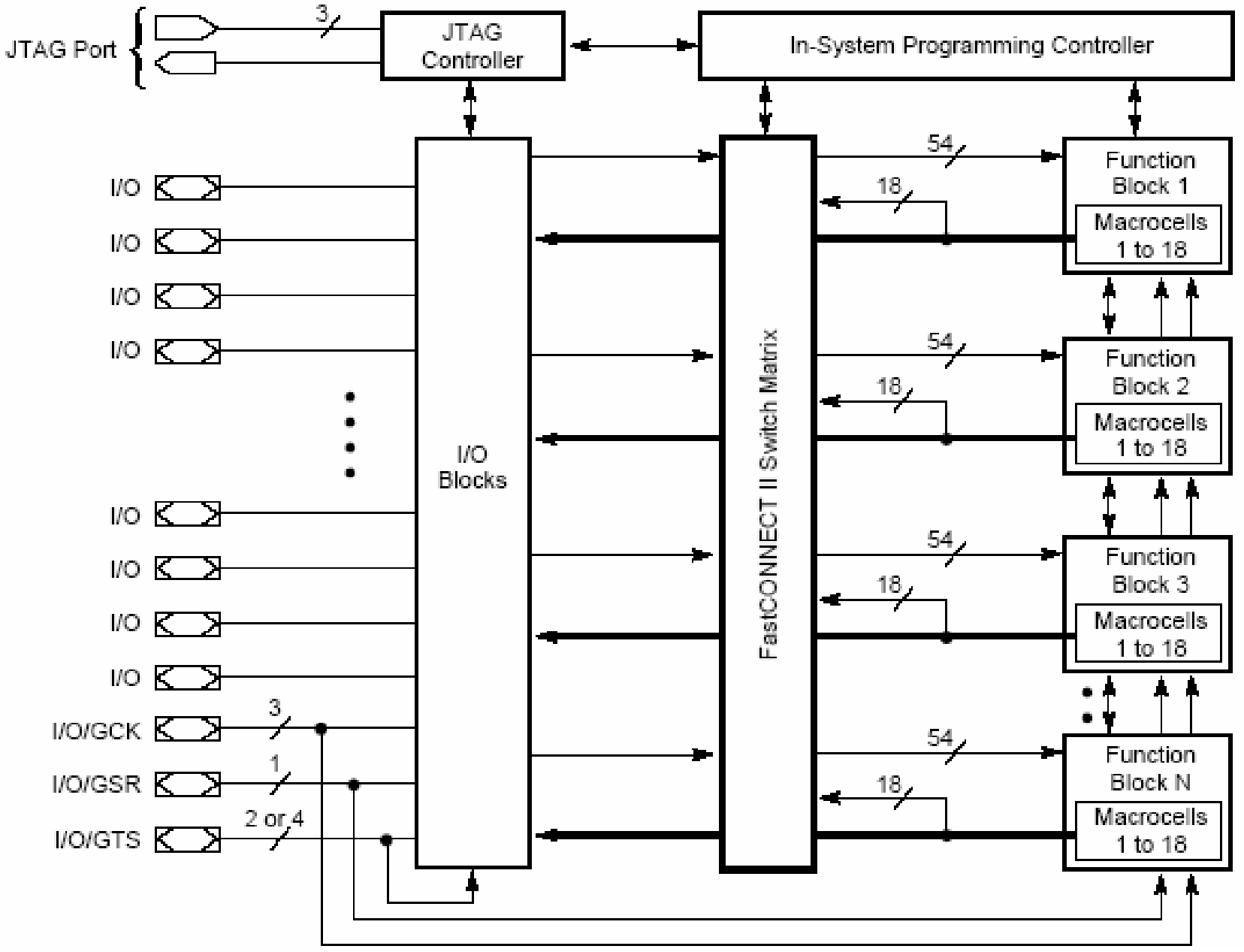
General CPLD configuration

I/O Blocks provide the connection to IC pins.

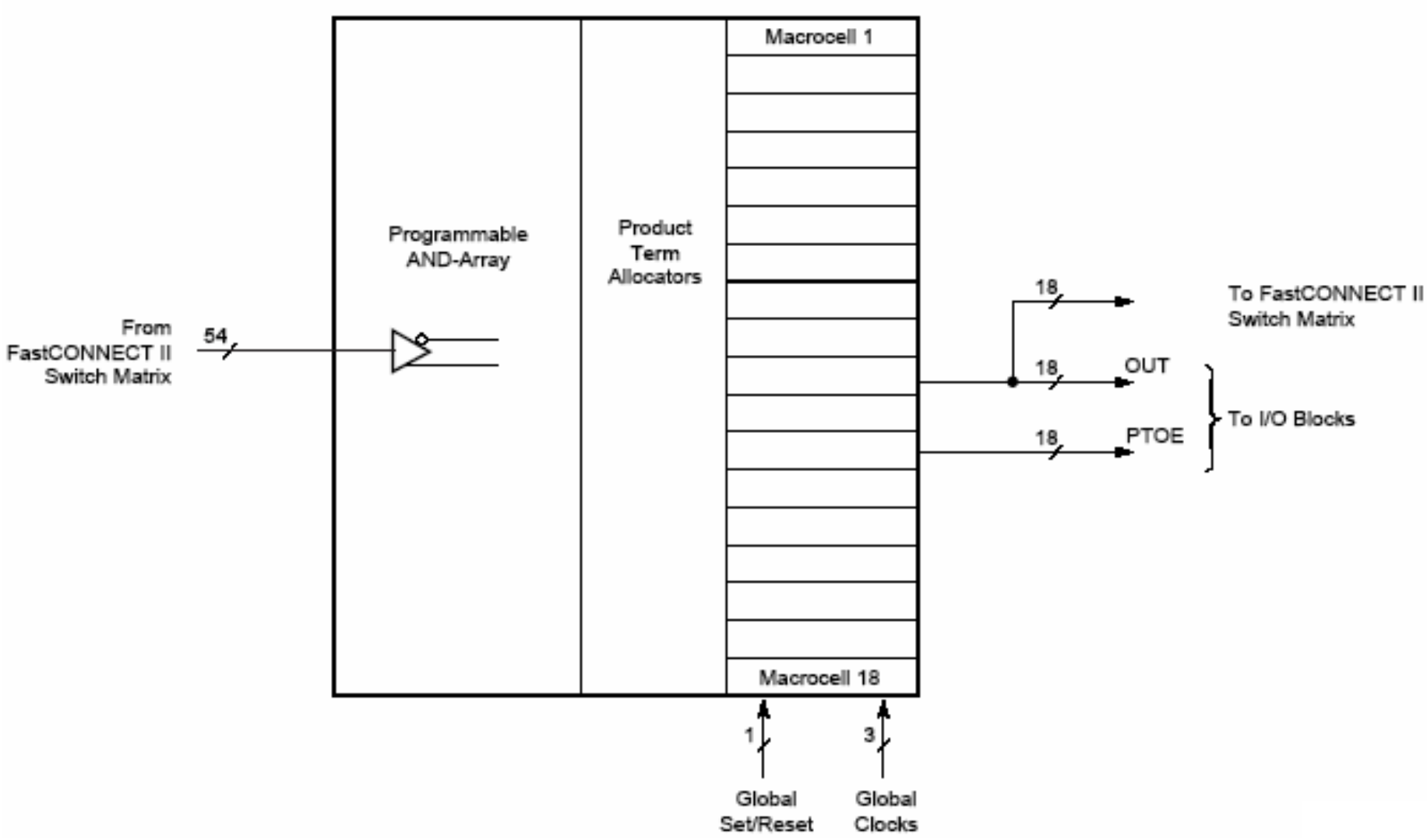
Complex Programmable Logic Devices - CPLD

- The switch matrix receives inputs from the I/O block and directs it to the individual macrocells;
- Similarly, selected outputs from macrocells are sent to the outputs as needed;
- Each PLD typically contains from 8 to 16 macrocells;
- The macrocells within each PLD are usually fully connected. If a macrocell has unused product terms they can be used by other nearby macrocells;
- Different manufacturers use different approaches to make individual PLDs (sometime called *function blocks - FB*), the type of macrocell, I/O blocks and the programmable interconnection structure.

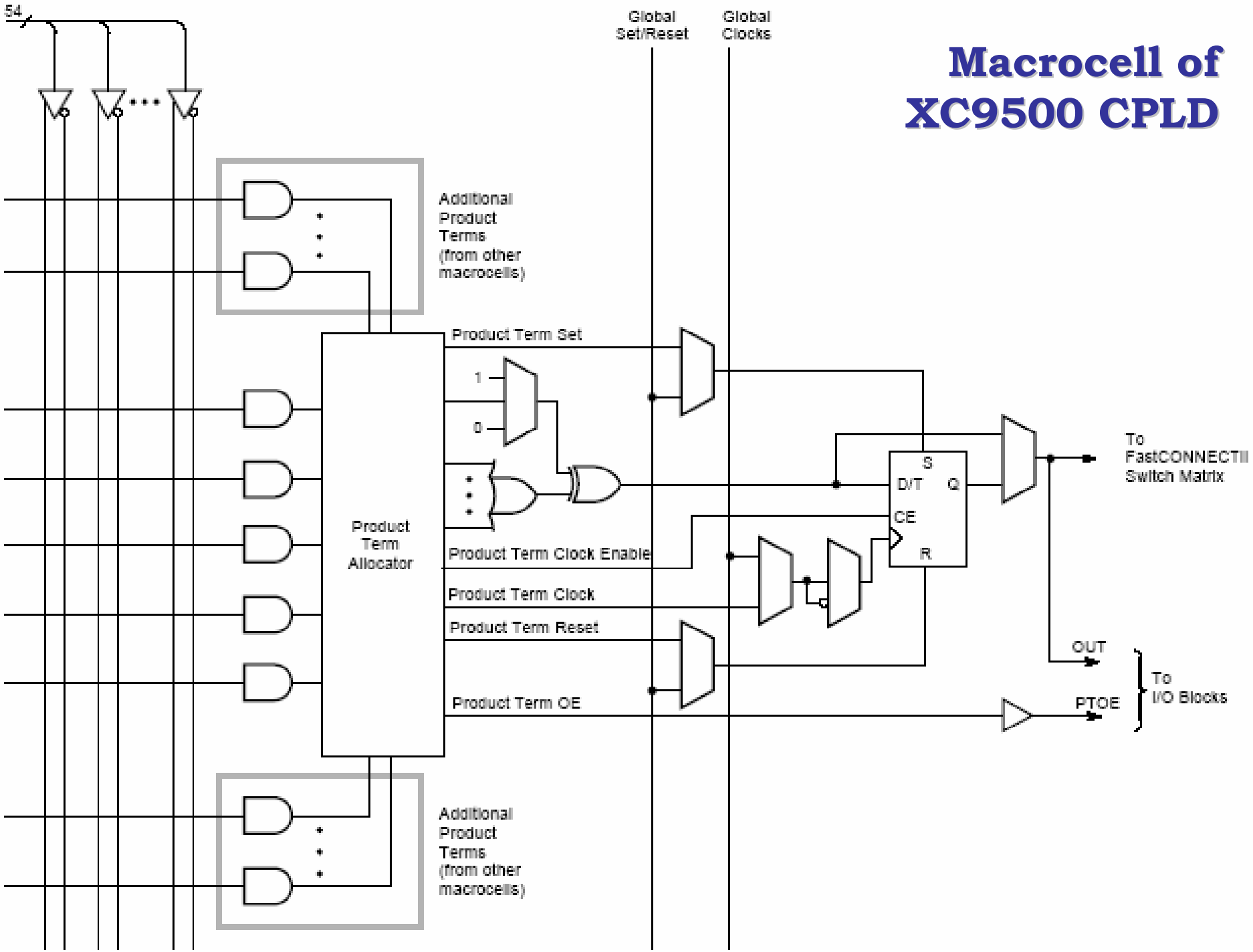
XILINX CPLD XC9500 Architecture

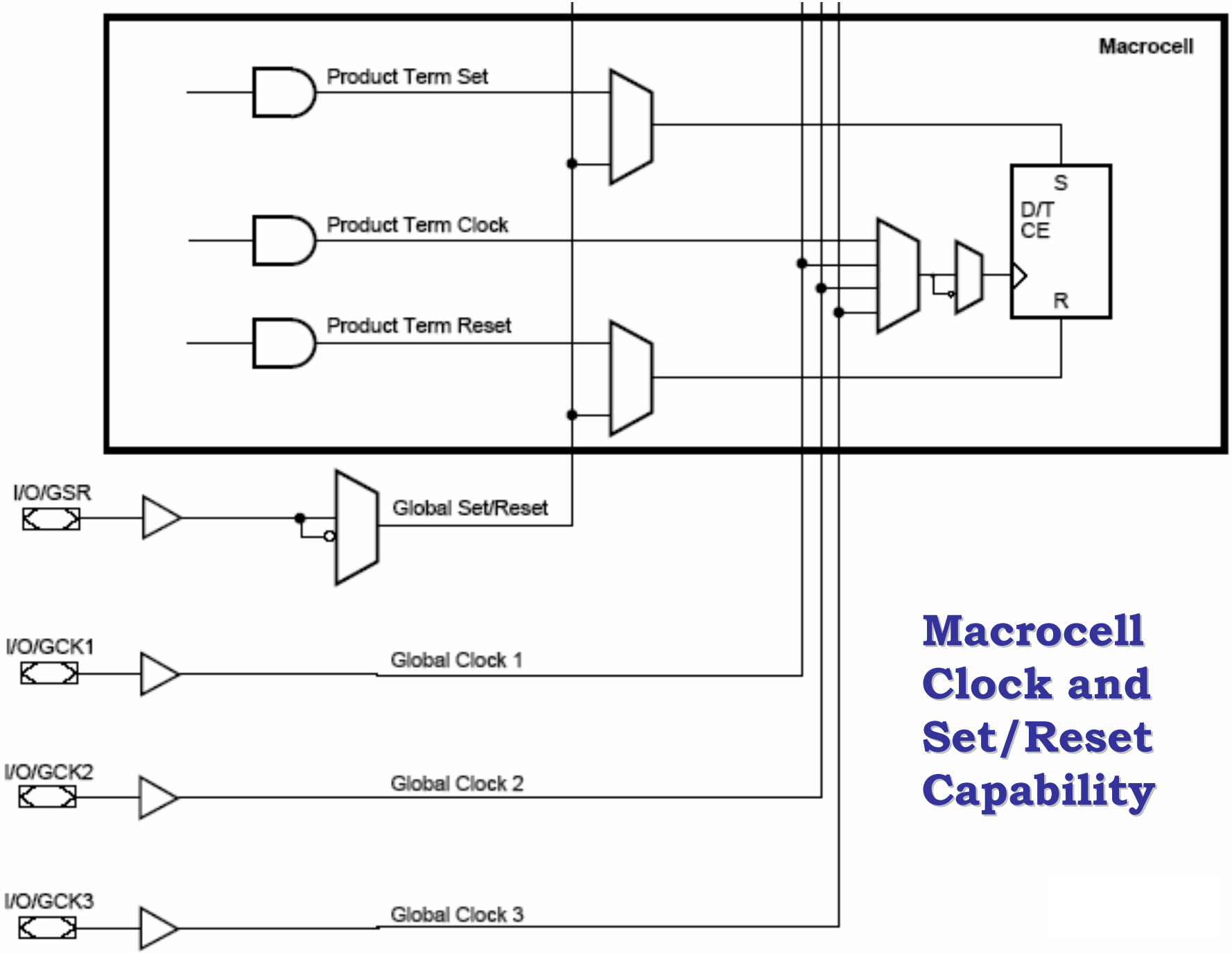


Function Block - FB



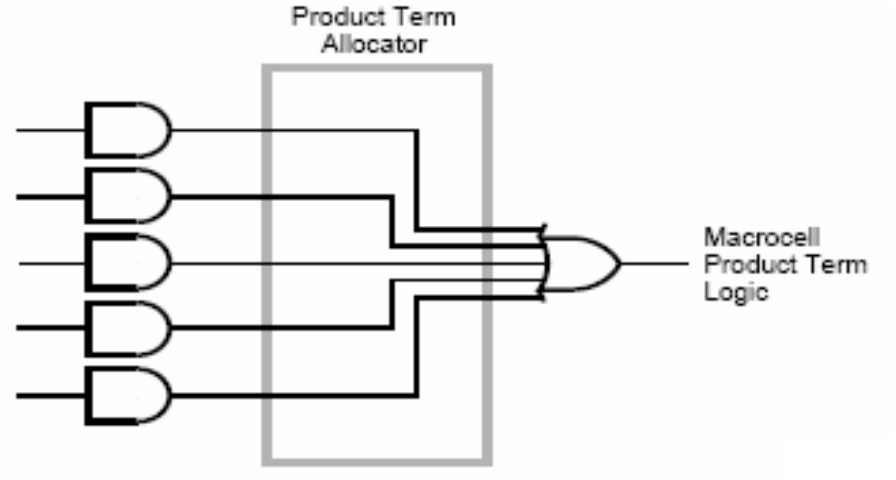
Macrocell of XC9500 CPLD

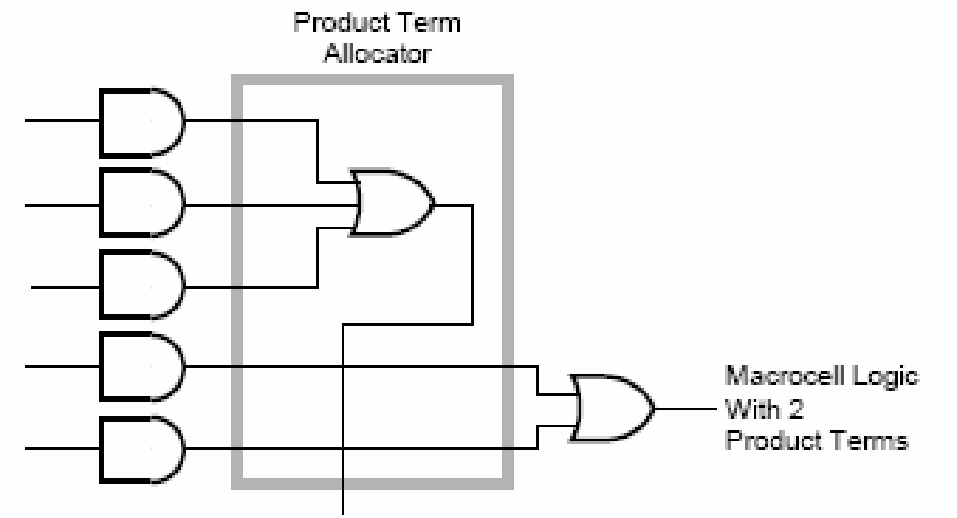


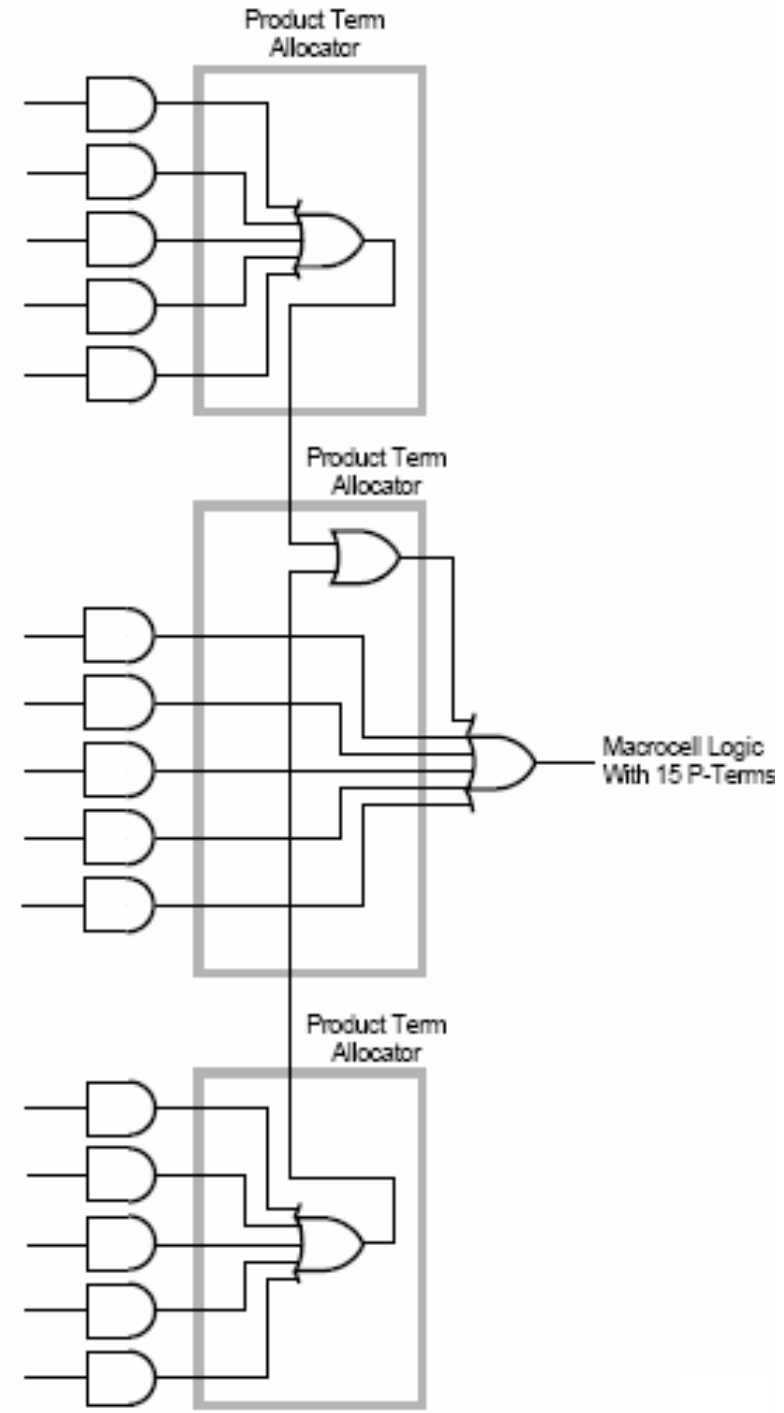


Macrocell Clock and Set/Reset Capability

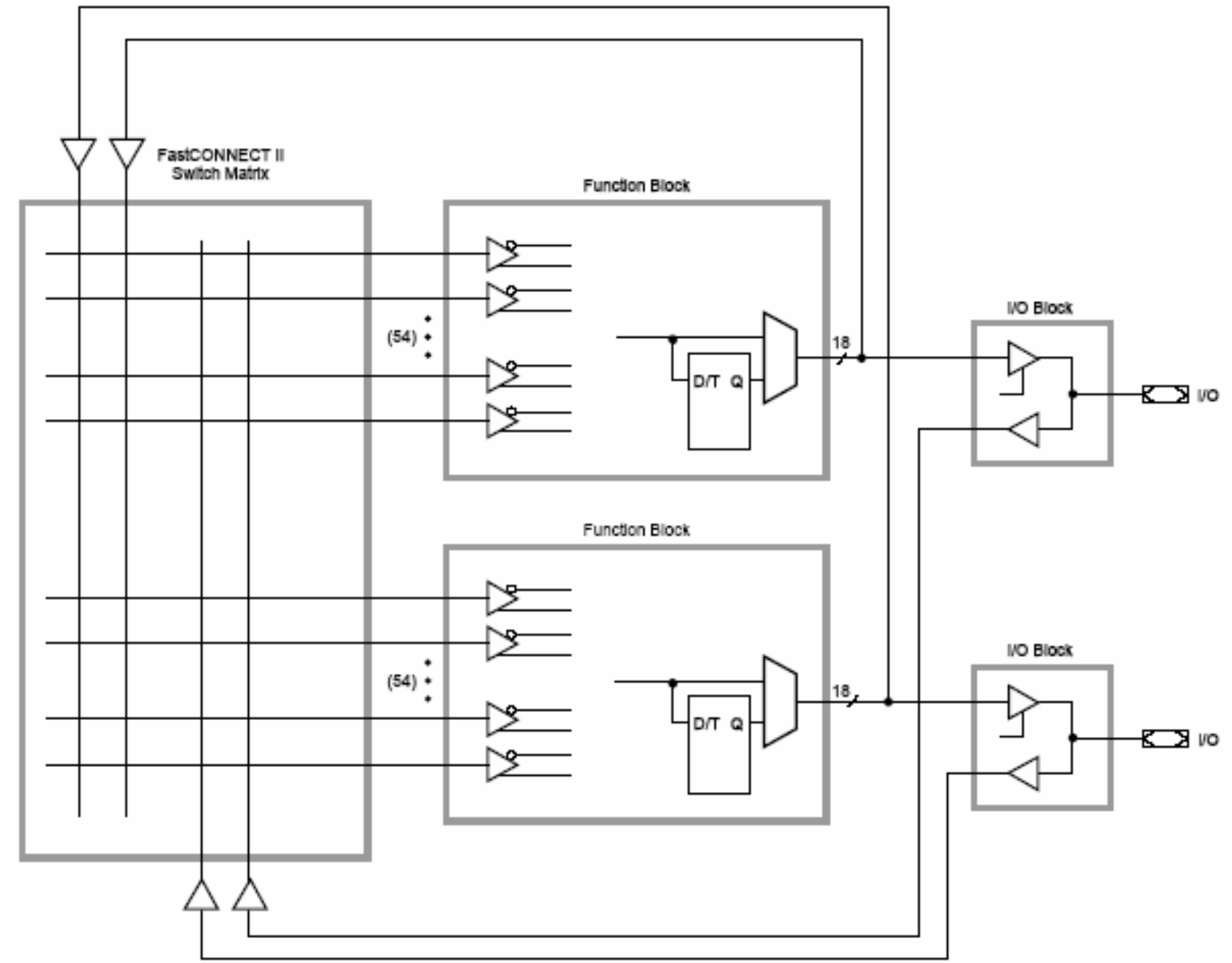
Product Term Allocator



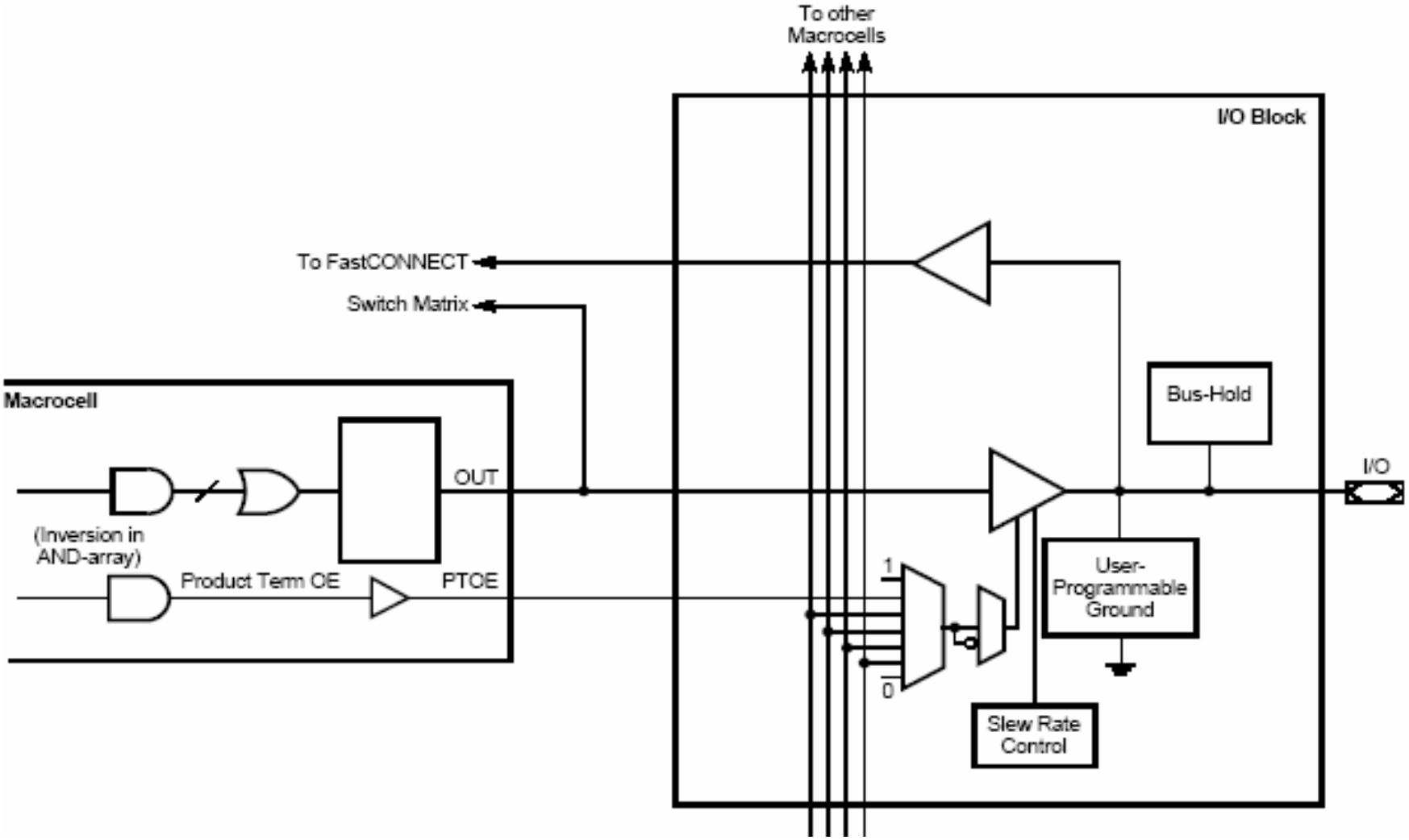




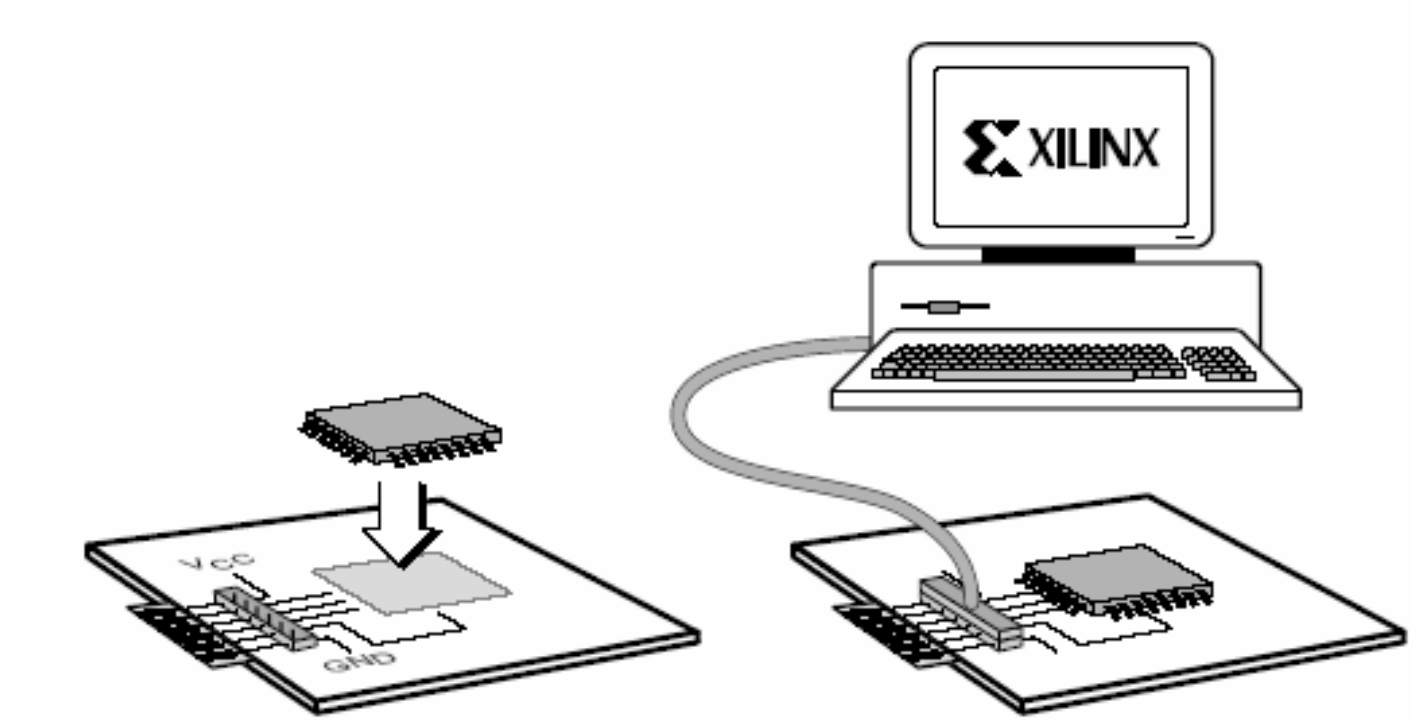
FastCONNECT II Switch Matrix



I/O Block - IOB


To other Macrocells
I/O Block
To FastCONNECT
Switch Matrix
Macrocell
OUT
(Inversion in AND-array)
Product Term OE
PTOE
Bus-Hold
I/O
1
0
User-Programmable Ground
Slew Rate Control

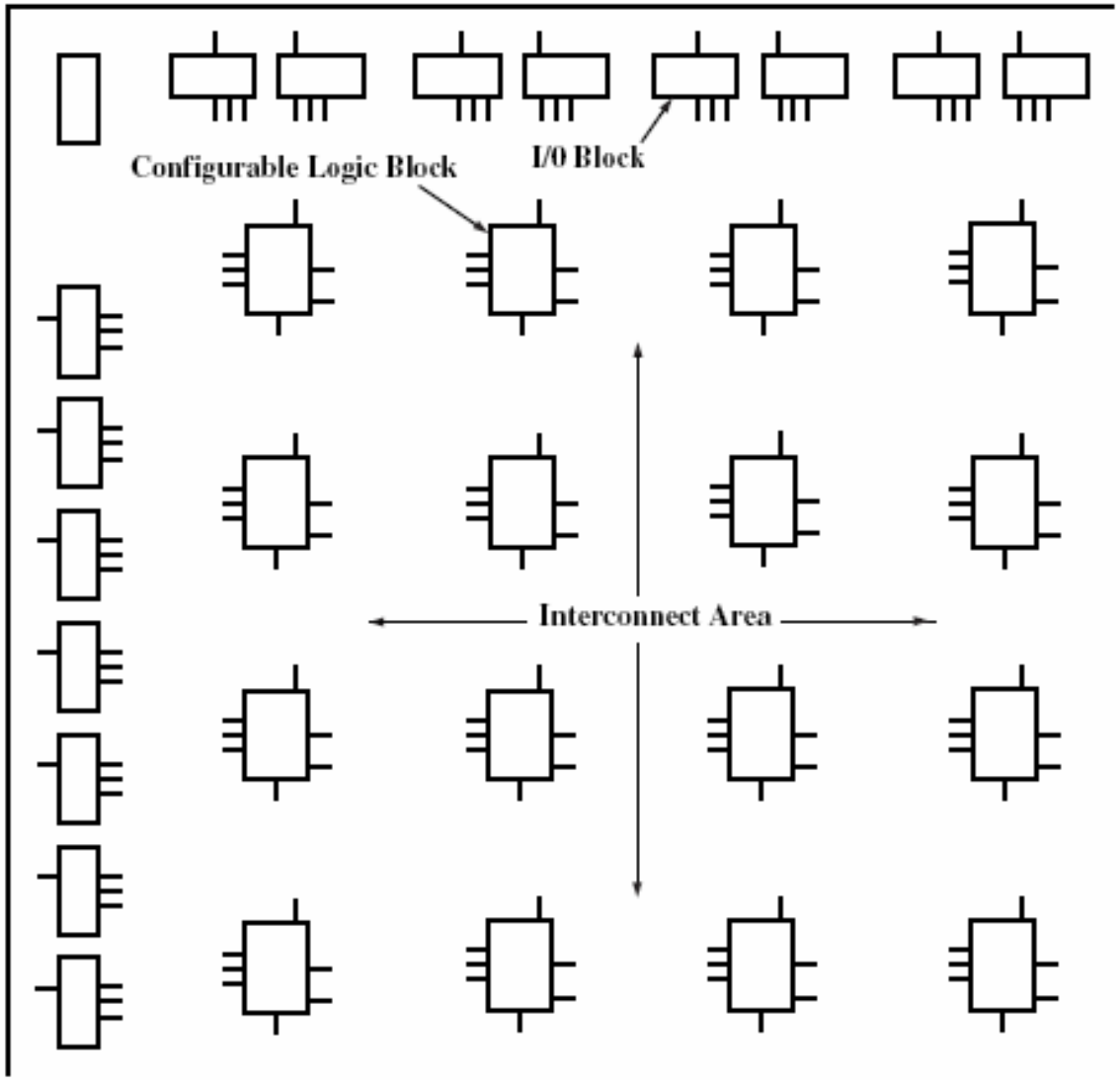
ISP



Field Programmable Gate Arrays - FPGA

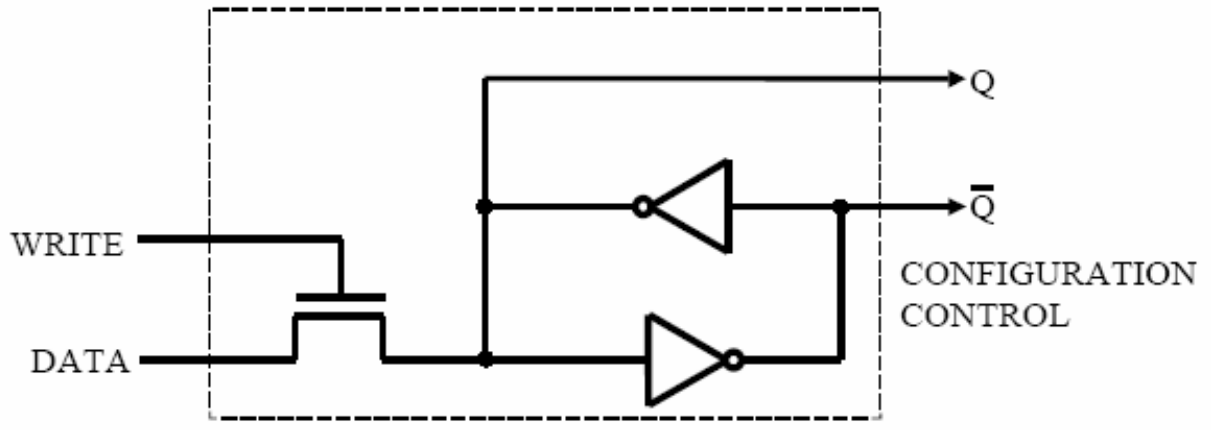
- The basic component used in ***VLSI*** design is the ***gate array***. A gate array consists of pattern of gates fabricated in an area of silicon that is repeated thousands of times until the entire chip is covered with the gates;
- A typical programmable gate array (PGA) is an IC that contains an array of identical logic cells with programmable interconnections. The user can program the functions realized by each logic cell and the connections between cells. Such PGAs are often called FPGAs since they are field-programmable.
- A typical FPGA consists of an array of hundreds or thousands of logic blocks, surrounded by programmable input and output blocks and connected together via programmable interconnections.

XILINX XC3020
Logic Cell Array (LCA)



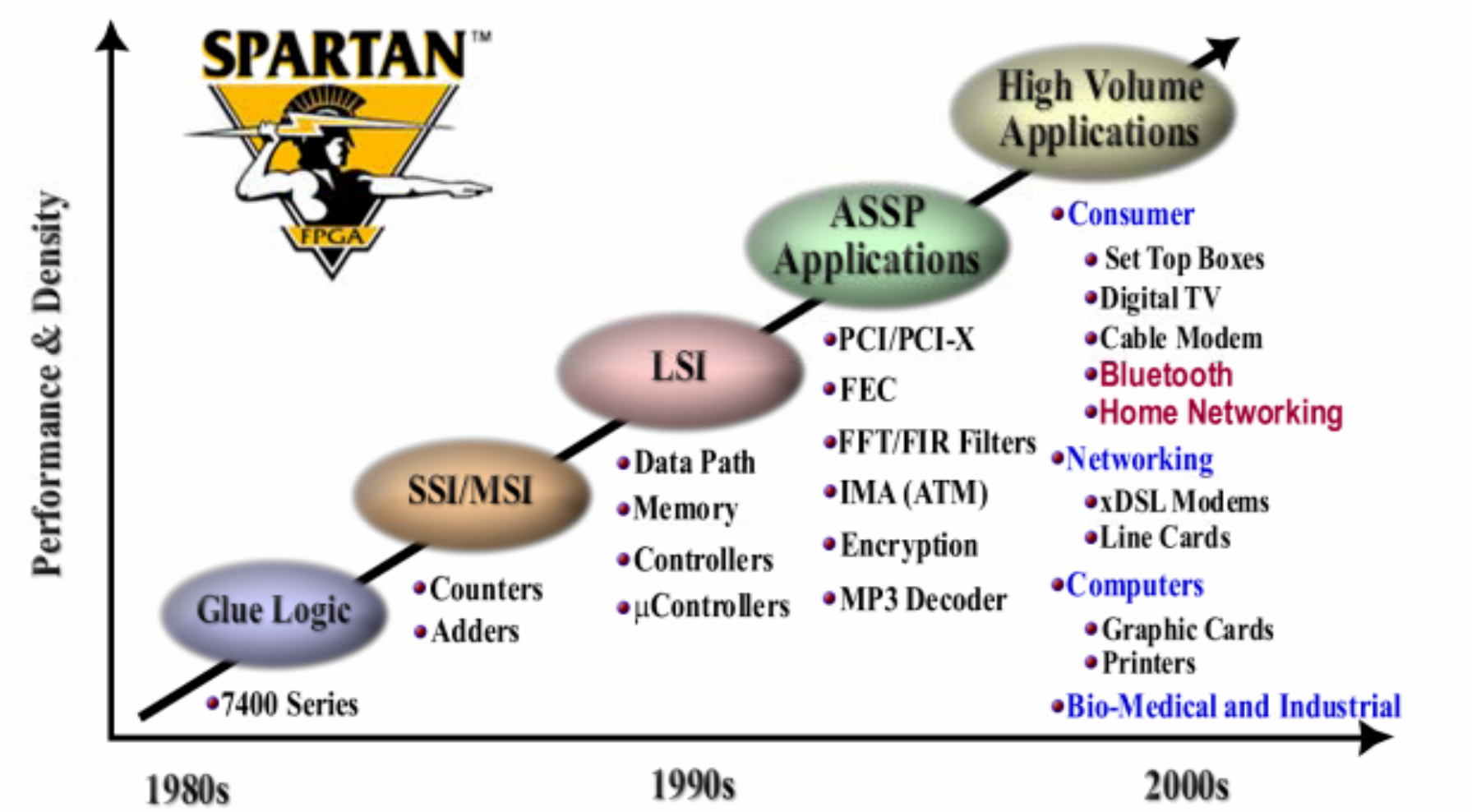
The interconnections between these blocks can be programmed by storing data in internal configuration memory cells.

Configuration Memory Cell

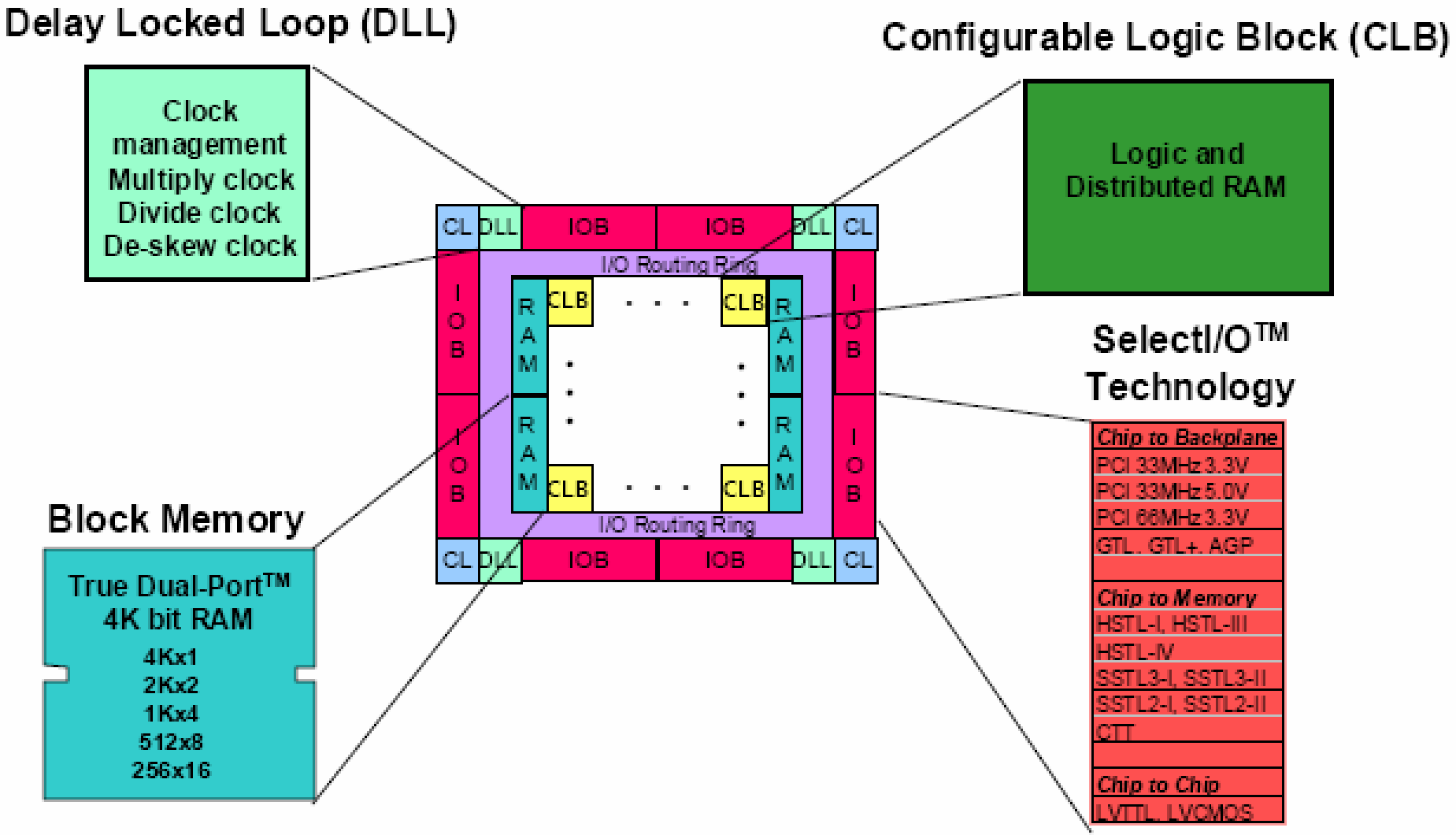


The configuration memory cells are programmed after power has been applied and logic function and interconnections are retained until the power exists. During configuration, when a WRITE signal is applied to the pass transistor, DATA is stored in the cell. Each connection point in the LCA has an associated memory cell, and the data stored in that cell determines whether the connection is made or not.

FPGA Application Trends



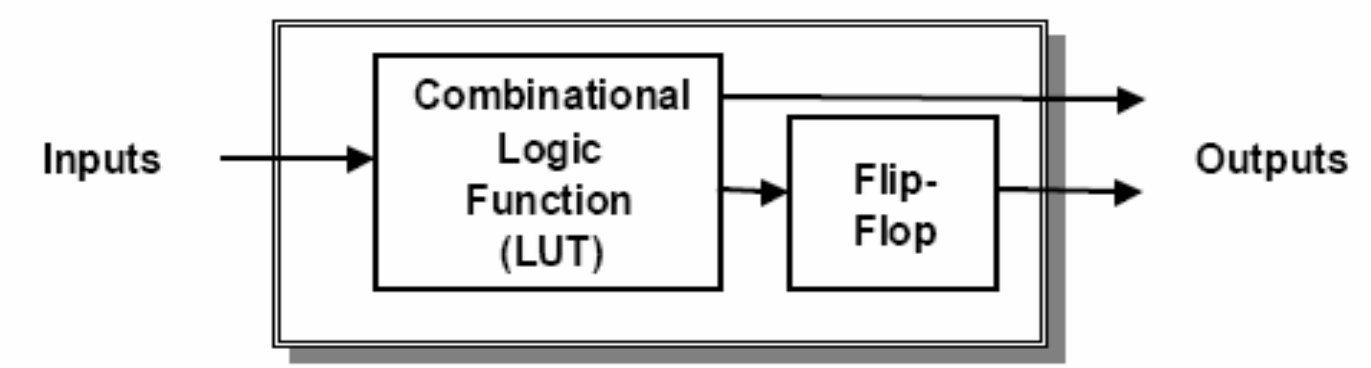
Top-level Architecture of Present Generation Xilinx FPGA



Top-level Architecture of Present Generation Xilinx FPGA

- Configurable logic blocks (CLBs)
  – Implement logic and memory here!
- I/O blocks
  – Communicate with other chips
  – Choose from 16 signal standards
- Block RAM
  – On-chip memory for higher performance
- Clocks and delay locked loops (DLLs)
  – Synchronize to clock on and off chip
- Rich interconnect resources
  – Three-state internal buses

Configurable Logic Blocks - CLB



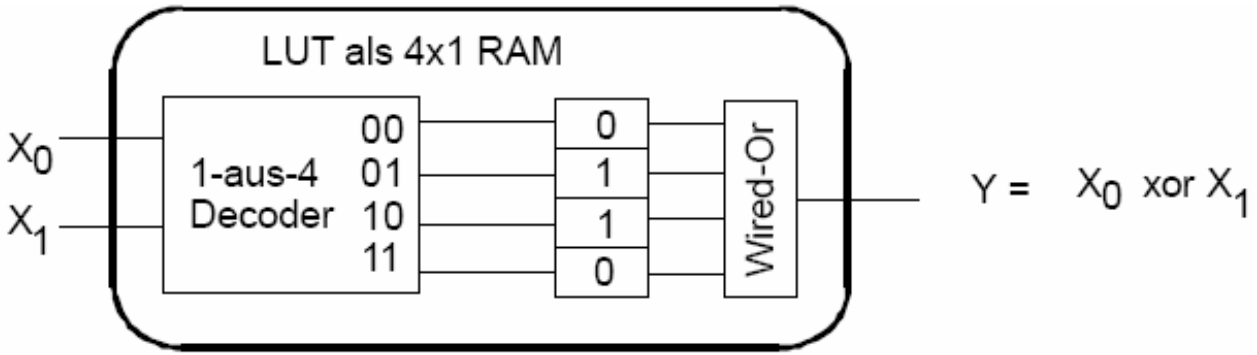
- Combinational logic generated in a lookup table (LUT)
  – Any function of available inputs

Generates any function of its inputs

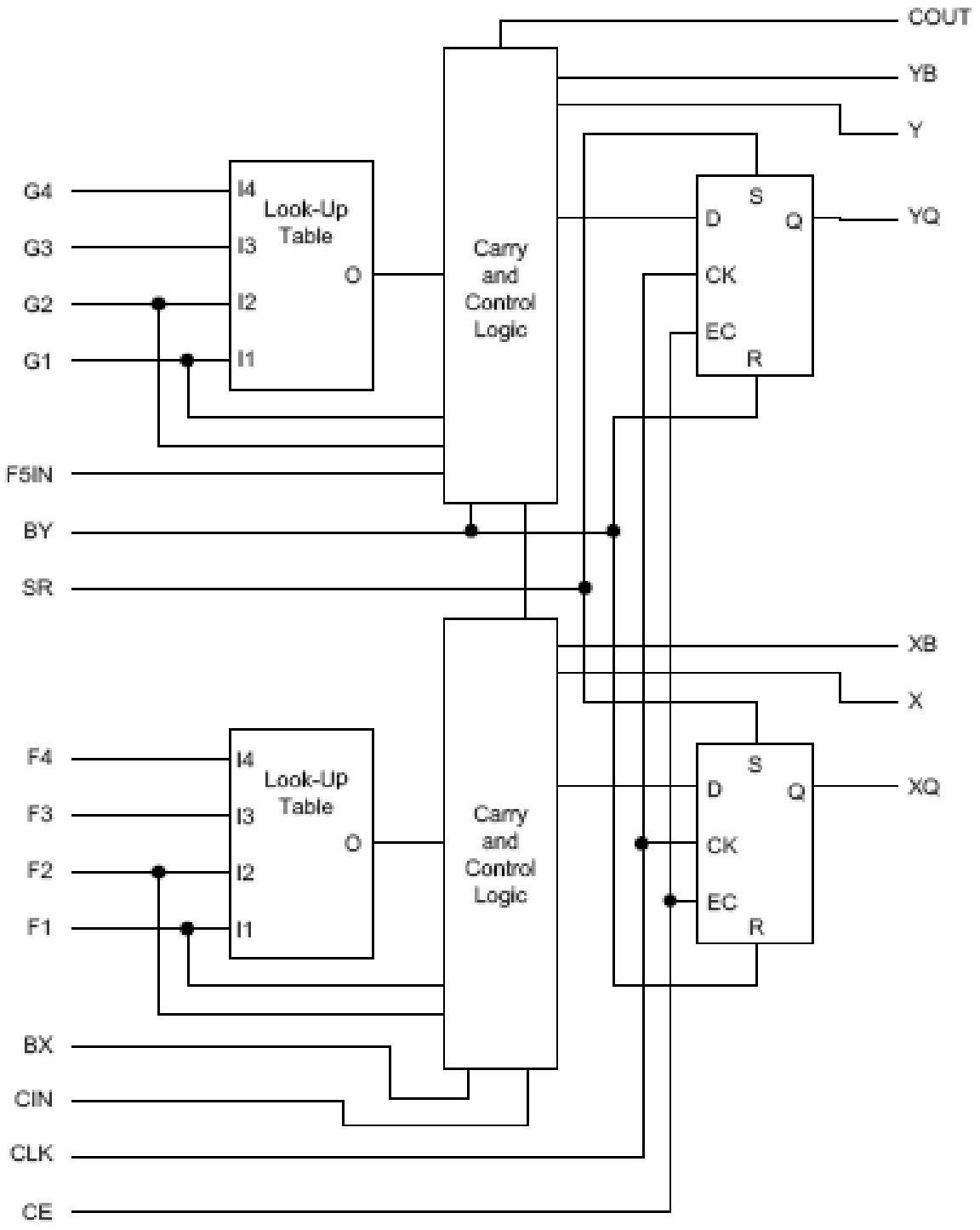
– Typically 4 inputs

- Logically equivalent to a 16x1 ROM

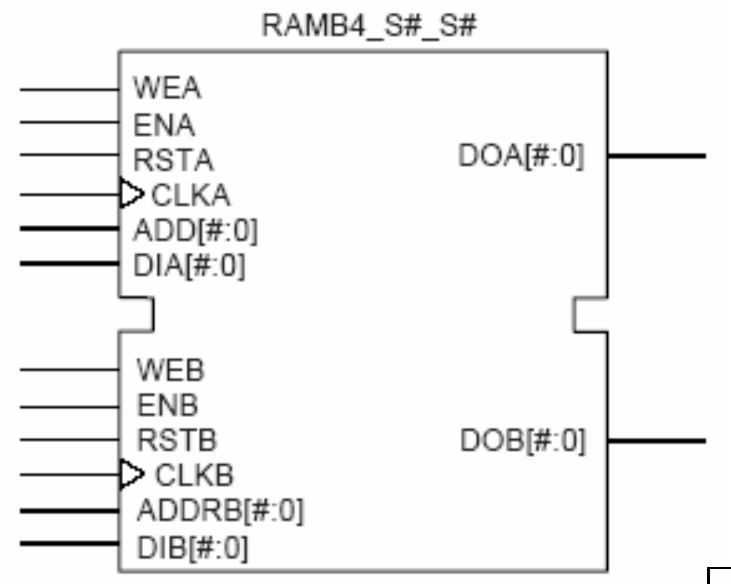
Inputs	Output
0000	0
0001	1
0010	1
0011	0



CLB – Slice (2 LC)

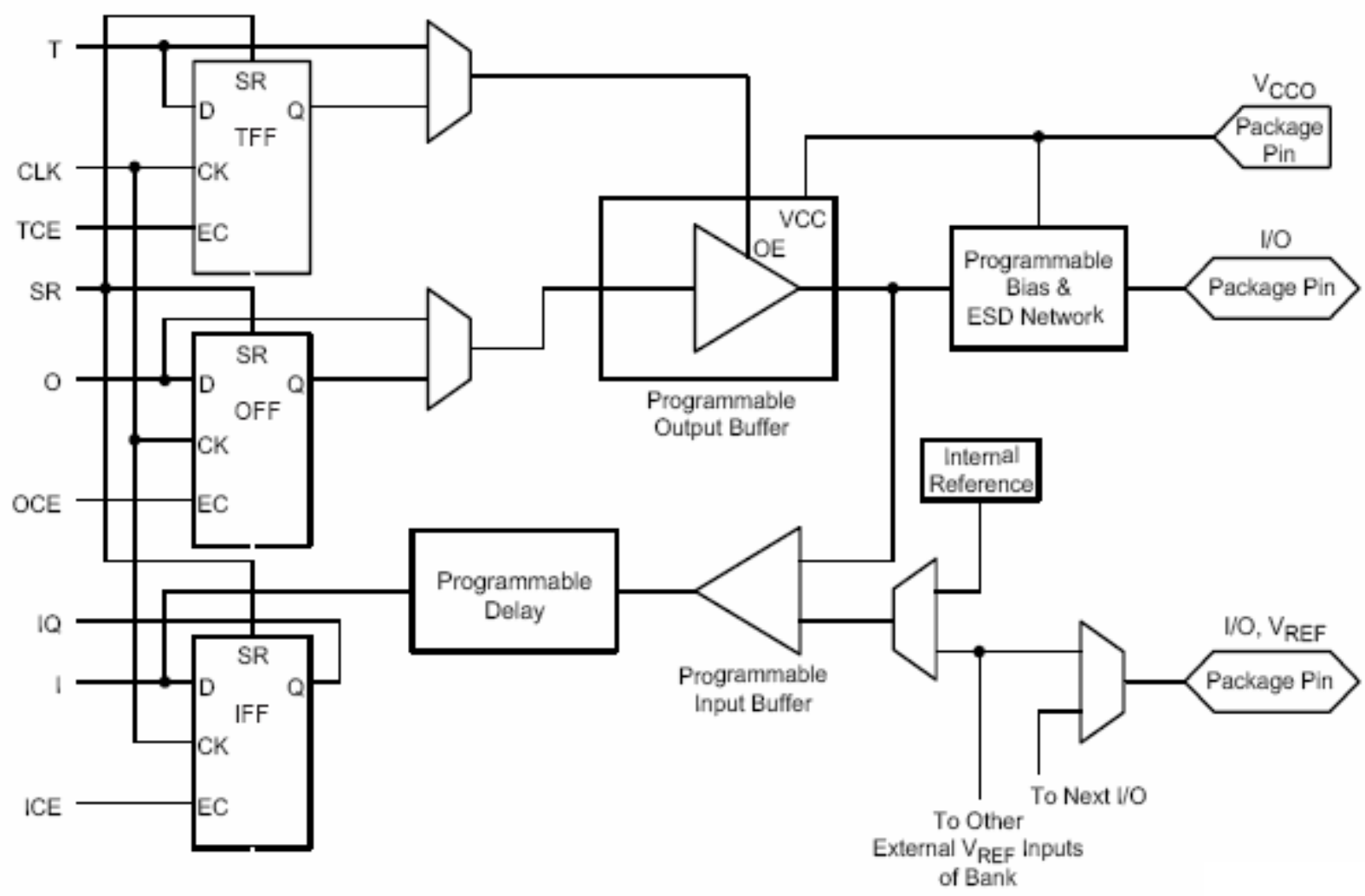


Block RAM



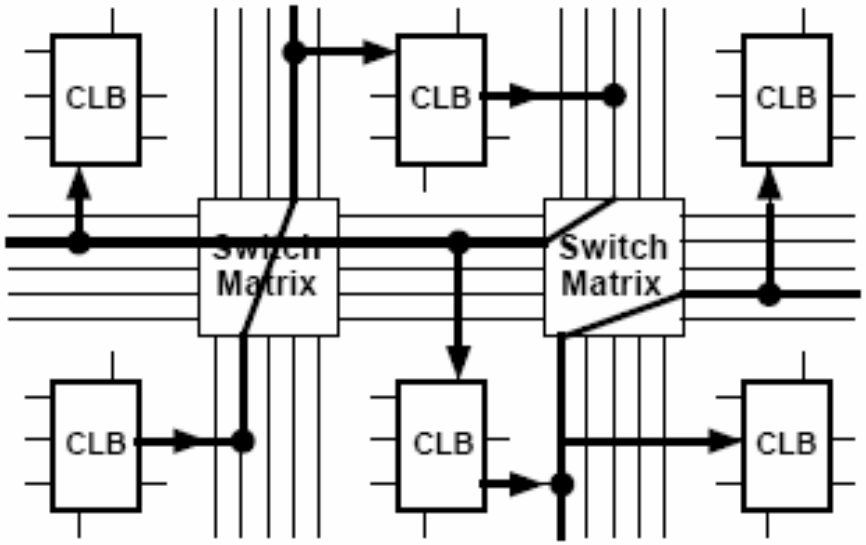
Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

I/O Block - IOB

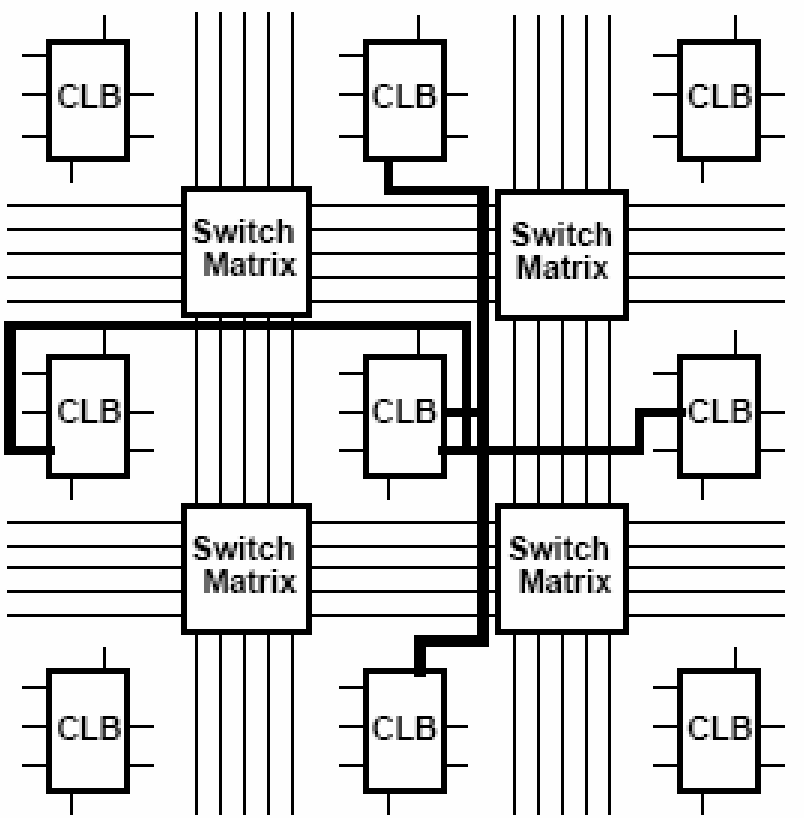

T
CLK
TCE
SR
O
OCE
IQ
I
ICE
SR
D
Q
TFF
CK
EC
SR
D
Q
OFF
CK
EC
SR
D
Q
IFF
CK
EC
VCC
OE
Programmable
Output Buffer
VCCO
Package
Pin
Programmable
Bias &
ESD Network
I/O
Package Pin
Internal
Reference
Programmable
Delay
Programmable
Input Buffer
I/O, VREF
Package Pin
To Next I/O
To Other
External VREF Inputs
of Bank

Programmable Routing Matrix

General-purpose Interconnects

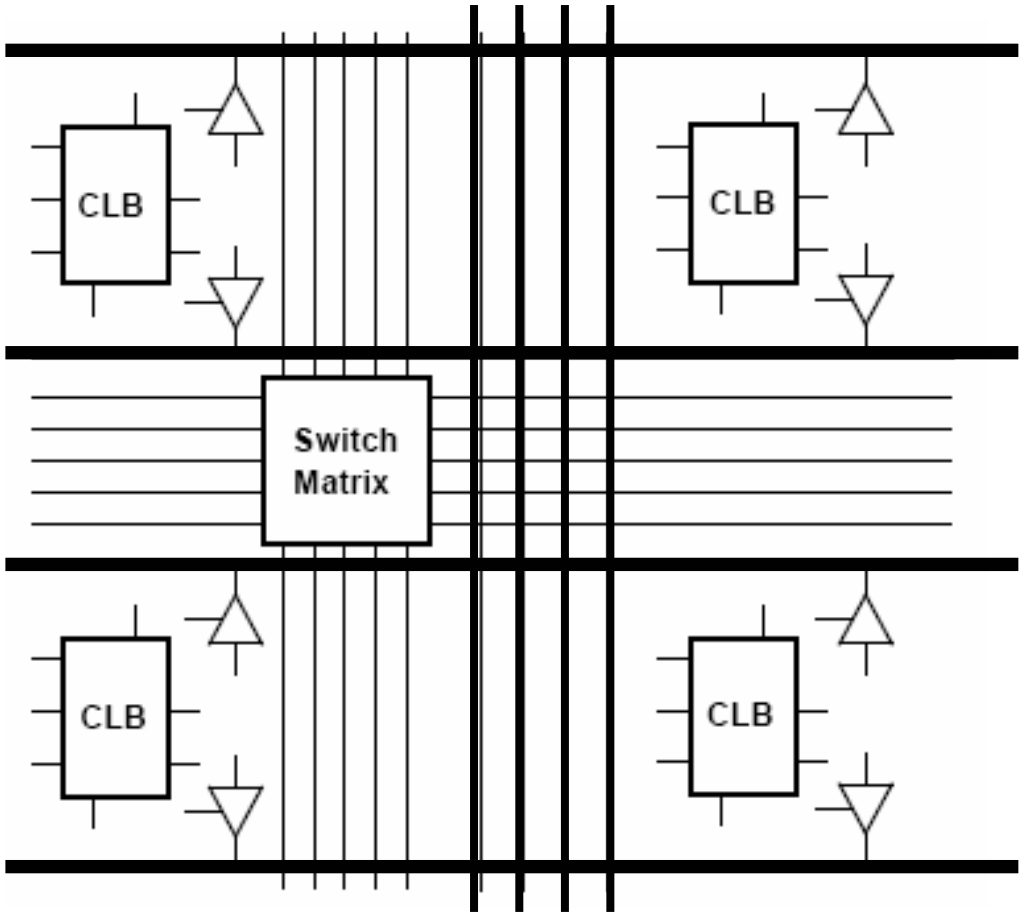


Direct Interconnects Between Adjacent CLBs



Programmable Routing Matrix

Vertical and Horizontal Long Lines



Hersteller von PLD

Hersteller	PLD	CPLD	FPGA
Actel (incl. Gatefield)			SX/SX-A-Familie MX-Familie ProASIC-Familie eX-Familie
Altera		MAX7000-Familie MAX9000-Familie	FLEX6000-Familie FLEX10K-Familie APEXII-Familie APEX20K-Familie
Atmel	PAL-kompatible SPLD	ATF-Familie	AT40K-Familie AT94K-Familie
Cypress	PALCE	Delta39K Ultra37K Flash370i	
Lattice (Vantis von AMD)	ispGAL GAL SPLD	5000-Familie ispMACH4A 2000-Familie 8000-Familie	
Lucent			ORCA-Familie
Quicklogic			pASIC-Familie Eclipse-Familie
Xilinx		XC9500 CoolRunner	VIRTEX-Familie Spartan-Familie XC5000-Familie XC3000-Familie XC5200-Familie